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THESIS

**DESIGN OF DISCRETE TIME RADIO RECEIVER FOR
THE DEMODULATION OF POWER-SEPARATED CO-
CHANNEL SATELLITE COMMUNICATION SIGNALS**

by

Brian D. Slosman

September 2013

Thesis Advisor:
Second Reader:

Frank Kragh
Scott Matey

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Several commercial companies are offering satellite modulators and demodulators that allow frequency reuse over satellite communications links. There are two methods to demodulate these co-channel signals. The first method requires *a priori* knowledge of one of the two signals linearly superimposed in the satellite downlink. With this knowledge, the known signal is cancelled using subtraction to reveal the unknown co-channel signal.

A second method of recovering both signals is possible if adequate power separation of the two signals allows recovery of the strong signal. After recovery of the strong signal, the data can be re-modulated and then cancelled from the composite signal to reveal the weak signal. This method has the advantage of not requiring *a priori* information which widens the applications for layered modulation techniques to simplex, broadcast, and multi-cast network architectures.

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DEMODULATION OF POWER-SEPARATED CO-CHANNEL SATELLITE
COMMUNICATION SIGNALS**

Brian D. Slosman
Major, United States Army
B.A., University of Maryland–College Park, 1995

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September 2013**

Author: Brian D. Slosman

Approved by: Frank Kragh, PhD
Thesis Advisor

Scott Matey, Lieutenant Colonel, United States Army
Second Reader

R. Clark Robertson, PhD
Chair, Department of Electrical and Computer Engineering

Rudy Panholzer, PhD
Chair, Space Systems Academic Group

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LIST OF ACRONYMS AND ABBREVIATIONS

ACM	Adaptive Coding and Modulation
AGC	Automatic Gain Control
BER	Bit Error Ratio
BPSK	Binary Phase Shift Keying
DDS	Direct Digital Synthesizer
DVB-S2	Digital Video Broadcasting-satellite, Second Generation
8PSK	8-Phase Shift Keying
GTED	Gardner Timing Error Detector
HP	High Power signal, in layered modulation
IID	Independent and Identically Distributed
ITU	International Telecommunications Union
LDPC	Low Density Parity Check
LP	Low Power signal, in layered modulation
MF	Matched Filter
NRZ	Non-Return to Zero
PCMA	Paired Carrier Multiple Access
PD	Phase Detector
PLL	Phase Lock Loop
PSD	Power Spectral Density
QPSK	Quadrature Phase Shift Keying
SCADA	Supervisory Control and Data Acquisition
SNR	Signal to Noise Ratio
SRRC	Squared Raised Root Cosine
TWTA	Traveling Wave Tube Amplifier
VSAT	Very Small Aperture Terminal
VCM	Variable Coding and Modulation
VoIP	Voice over Internet Protocol
ZCTED	Zero Crossing Timing Error Detector

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EXECUTIVE SUMMARY

Commercial satellite communication companies, such as ViaSat and Comtech EF Data, have been aggressively marketing the use of layered modulation. Layered modulation is a technology that allows two or more satellite communications ground sites in the same uplink and downlink coverage beams to use the same uplink frequencies to communicate. The result of multiple uplink signals at the same frequencies is a composite signal at the satellite transponder and, therefore, in the downlink. This composite signal is a linear superposition of the uplink signals, or the additive sum of those signals. The ground sites subsequently separate the signals in the composite signal to obtain their desired signal(s). This technology allows the reuse of satellite bandwidth. This bandwidth reuse presents many advantages. The key advantage is a reduction in the space segment costs of operating a satellite communications link [1]. For example, this technique has found primary application in the point-to-multi-point communications of very small aperture terminal (VSAT) networks. In these networks, the central hub of the star topology network produces a wideband signal to provide high data rate communications through a forward link to the remote terminals. The remote terminals produce a narrow bandwidth, low data rate return link to the hub. Traditionally the hub's forward link and the terminals' return links would be separated by frequency. Using layered modulation the return links can be placed within the same frequency band as the hub's signal, resulting in a bandwidth savings to the network operator. This concept is graphically depicted in Figure 1. The challenging part of this technology is in the separation of the composite signal into the initial signals at the receivers. One of the methods of separating this signal is the subject of this research.

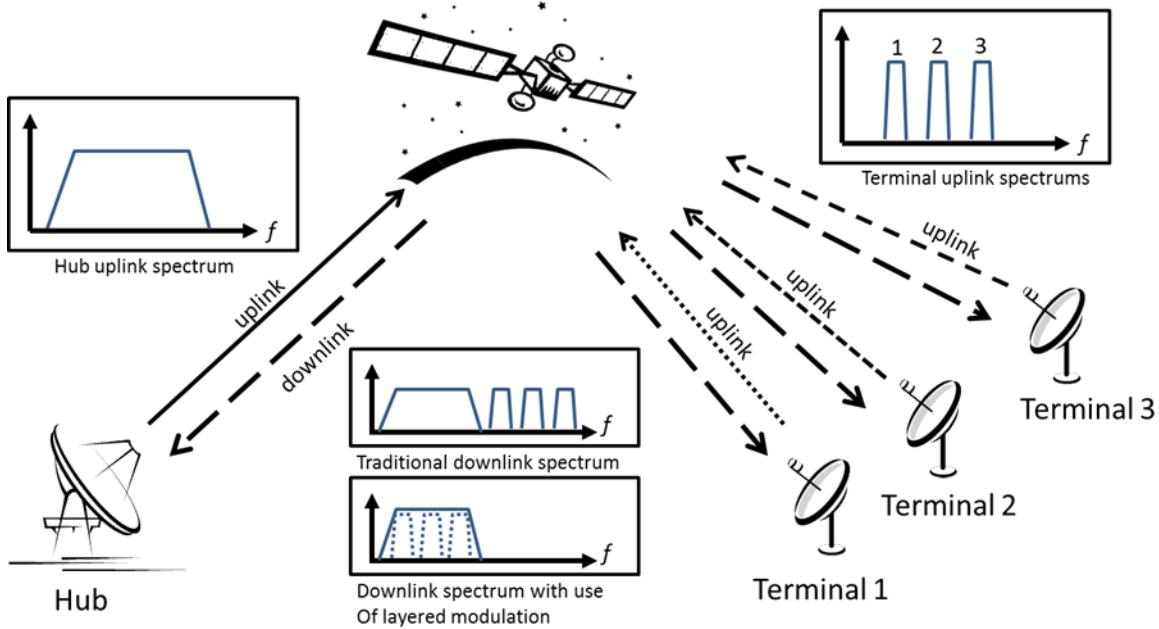


Figure 1. An example of the bandwidth savings possible with layered modulations.

When the composite signal returns in the downlink, there are two methods to recover the desired signal(s) [2]. The first method, currently employed by the above companies, is for each ground site to retain a copy of its outbound transmission and use a delayed and filtered version of this signal to cancel, or subtract, that signal's contribution to the composite signal in order to reveal the other signal(s). This method relies on the availability of the one of the signals *a priori*. In the second method, a satellite communications receiver successively demodulates the signal. The receiver first demodulates the higher powered of the two, or more, signals. The receiver then modulates the data and filters the resulting signal to produce a replica of the higher powered signal to use in a cancellation circuit. This second method relies on an adequate power separation between the high powered signal and the low powered signal(s) to mitigate the co-channel interference of the lower powered signal(s) on the high-powered signal. The signal flow for both of these methods is shown in Figure 2. The second method of recovering the low powered signal(s) through successive demodulation is the subject of this research.

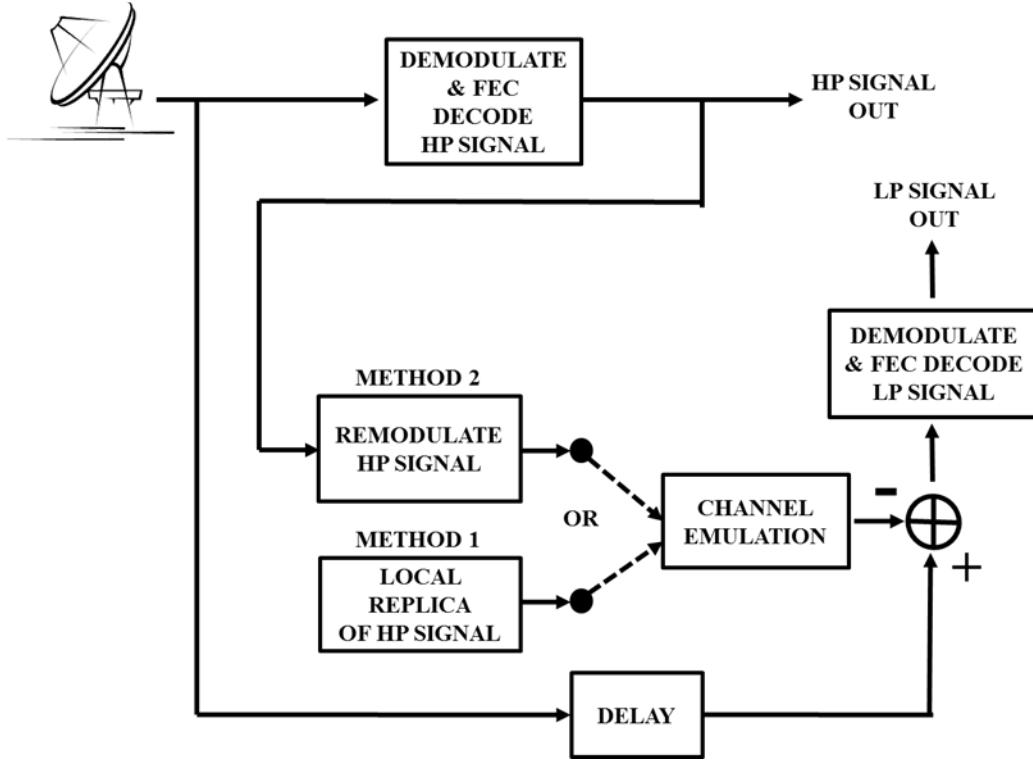


Figure 2. Signal flow for both methods of separating layered modulation signals.

The second method of recovering the desired signal(s) from the super-positioned signal has received significantly less attention in research. The advantage of this method is that the receiver does not need *a priori* knowledge of the high powered signal. For applications such as network monitoring, signals intelligence, and broadcast, the receiver would not have *a priori* knowledge of any of the signals. It is for the benefit of these applications, and in order to identify additional applications, that additional research into the performance of successive demodulation must be studied.

In this research, a methodology is presented to better understand the performance of the second method in the demodulation of power-separated co-channel satellite communications signals. During the course of this research, we designed and modeled a QPSK discrete-time radio receiver in Simulink for use in continued research on this subject. Effort was expended in ensuring that this receiver is very realistic and representative of modern receivers. Specifically, the receiver was designed to operate without specific knowledge of the frequencies and phases of the transmitter's carrier

oscillator and timing clock. These aspects of coherent communications are addressed in the inclusion of a carrier frequency/phase synchronization circuit and a symbol timing synchronization circuit. The creation of these two circuits consumed a large portion of the conducted research.

In the end, this research concludes with an initial design of a representative discrete-time QPSK receiver. The performance of this receiver was tested in relation to the bit error rate (BER) performance of the ideal QPSK demodulator. The result of this testing is that the receiver performs at very close to optimum levels, even with realistic parameters on the precision of both transmitter and receiver oscillators and clocks. The application of this receiver in the conduct of the suggested follow-on research was demonstrated with a simulation of the impact of co-channel interference in the initial demodulation of a high-powered layered modulation signal. The results of this simulation are in agreement with other research on the subject and demonstrate the utility of the receiver in continued research on this subject.

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- [1] ViaSat, “PCMA – Paired Carrier Multiple Access,” ViaSat, Carlsbad, 2008.
- [2] S. Skjei, “Re-Using Satellite Bandwidth,” in PBS TechCon, Las Vegas, 2009.

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I. INTRODUCTION

Since the origins of satellite communications, there has been a consistent demand for increased capacity for the communications possible through this medium. This trend of increasing demand for capacity has resulted in some novel technologies aimed at increasing the capacity possible with a set bandwidth. Two of the technologies for increasing capacity with a set bandwidth are grouped under the term bandwidth reuse and include hierarchical modulation and layered modulation [1]. The design of a representative discrete-time radio receiver with which to study and analyze the performance of one of two particular methods for demodulating layered modulation signals is documented in this thesis. A quick survey of the trend to increase capacity, with recent examples, a brief discussion of the satellite bandwidth reuse technologies, and justification for the use of a discrete-time radio for this study is appropriate as an introduction.

In February 1945, Arthur C. Clarke described in a letter to the editor of *Wireless World* the potential use of an orbiting communications relay to provide worldwide communications:

An “artificial satellite” at the correct distance from the earth would make one revolution every 24 hours; i.e., it would remain stationary above the same spot and would be in optical range of nearly half the earth’s surface. Three repeater stations, 120 degrees apart in the correct orbit, could give television and microwave coverage to the entire planet [2].

In 1948, Claude Shannon published the fundamental equation from which much of the historical progress of communications can be measured. Shannon demonstrated that the capacity C of a communications channel was limited by the bandwidth B of the channel and signal-to-noise ratio S/N of the signal on that channel as [3]

$$C = B \log_2 \left(1 + \frac{S}{N} \right). \quad (1-1)$$

Since Clark and Shannon's two landmark historical concepts were introduced, satellite communications technology has progressed to the point that the Clarke orbit, now referred to as "geosynchronous/geostationary orbit" is so well utilized that slots and frequencies are closely and carefully managed by the International Telecommunications Union (ITU), an international agency under the United Nations. Both the orbital slot and the authorized frequency allocation are precious resources for government owned/operated satellites and commercially owned/operated satellites. As with any finite resource, it is imperative to maximize the effective use of satellite communication resources. The two most critical resources, as alluded to in Shannon's Equation (1-1), are channel bandwidth and signal power. To highlight this, the cost associated with leased satellite capacity are driven by a combination of factors including access locations, bandwidth, transponder power required, and the performance level of the transponder (low-noise transponders garner premium pricing) [4]. Pricing is driven by the potential capacity of the satellite transponder. ViaSat identifies the three key factors for satellite communication network costs: satellite segment cost, equipment cost, and operating costs [5]. Of these three factors, satellite segment costs (assuming leased satellite communications bandwidth) represent the largest cost as a result of their recurring nature and the premium placed upon these resources. The literally astronomic costs of communication satellite design, launch, and operation makes the option of building and operating a communications satellite reasonable for only large governments and commercial satellite communication system operators.

A. COST-EFFECTIVE USE OF SATELLITE COMMUNICATION BANDWIDTH

Much of the progress made in satellite communications can be understood as an overall effort to improve the cost effectiveness, e.g., to maximize the available capacity of communication satellites for a given cost. Three recent examples highlight this trend: the new satellite digital broadcast standard, a new high-capacity communications satellite, and the proliferation of Very Small Aperture Terminal (VSAT) networks [6].

The developments of communication standards such as Digital Video Broadcasting-satellite Second Generation (DVB-S2) highlight efforts to maximize the

capacity of satellite communications. DVB-S2 is a broadcast standard that is replacing the first generation standard DVB-S. DVB-S2 improvements include:

- Low density parity check (LDPC) codes, a more efficient forward error correction coding,
- Variable coding and modulation (VCM), and adaptive coding and modulation (ACM) modes which allow dynamic changes to both the modulation and error correction to maximize capacity.

The adoption of this new standard offers a 30% performance gain compared to the first generation standard, thus, partially meeting the increased capacity required for higher-definition video broadcasting [7].

ViaSat-1 (pictured in Figure 1), a high capacity Ka-band communications satellite went into service on 16 January 2012 as the highest capacity satellite in the world. It offers 134 Gbps of total throughput capacity. In a brief to students at the Naval Postgraduate School, Mark Dankberg, ViaSat Chairman, explained the driving emphasis for the design. Visually using Equation (1-1) he explained that the overarching design goal was to maximize the capacity per cost of the system [8]. The primary service for the ViaSat-1 satellite is high-speed internet connectivity with 12 Mbps downstream capacity providing coverage to 70% of the population of North America [9]. This service allows high-speed internet access to remote areas as well as high speed internet access inflight to several commercial airlines [8]. Key to this service is the incorporation of the concept of a VSAT network.



Figure 1. Artist's rendition of ViaSat-1, a high capacity communications satellite.
From [10].

Initially, VSAT networks were utilized to provide two-way narrowband communications between remote sites and a central network. The hallmark of the network is that the remote sites use small antennas, less than three meters in diameter. A common example is the VSAT networks that provide the communications for credit card purchase authorizations at fuel stations [6]. As the capacity of these networks increased, the market for these services expanded to include the creation of higher capacity network infrastructures that would not be heavily reliant on terrestrial infrastructure. With the increase in capacity, these networks became capable of offering voice over internet protocol (VOIP) services and an ever increasing data communications capability to a variety of ground sites including mobile (ground, maritime, and air), and fixed locations. VSAT networks offer many organizations the ability to extend their wide area networks to remote locations, to maintain an air-gapped internal network without the use of commercial internet, or to provide internal network connectivity to remote underserviced locations, as in industrial operations or public infrastructure services including Supervisory Control and Data Acquisition (SCADA) networks [6]. The popularity of these services is evident in the marketing analysis which led to the creation of ViaSat-1.

The pressures driving the increased capacity of satellite communication networks are analogous to those in the commercial terrestrial mobile communications networks

that resulted in the success of high-capacity fourth generation cell phone networks. Satellite bandwidth reuse is one of several technologies seeking to deliver on these requirements for greater capacity [1].

B. SATELLITE BANDWIDTH REUSE

Satellite bandwidth reuse refers to technologies which increase the data rate on a particular satellite communications link without increasing the bandwidth required to provide that additional capacity. Two such bandwidth reuse technologies are hierarchical modulation and layered modulation.

1. Hierarchical Modulation

Hierarchical modulations enable a satellite broadcast provider to implement new services while maintaining backwards compatibility to existing users [1]. This form of bandwidth reuse is ideally suited to networks with a large number of legacy receivers which want to add services without requiring adoption of new equipment. With hierarchical modulation, the additional capacity of a more spectral efficient modulation can be demodulated by the newer terminals but has the appearance of the old modulation type to the legacy terminals. An illustrative example is provided by Figure 2. An 8-phase shift keyed (8PSK) signal is seen by the legacy terminals as a QPSK signal. A newer terminal would receive an additional bit of information with each symbol compared to the legacy terminals, providing a 50 percent improvement in capacity. It must be noted that an actual 8PSK signal would have a better bit error ratio (BER) performance than the displayed hierarchical modulation due to the differences in the compression of the constellation points; i.e., the 8PSK constellation would not be compressed near the QPSK constellation points to maintain acceptable performance in the legacy terminals. This technology is used today by Sirius Satellite radio [1].

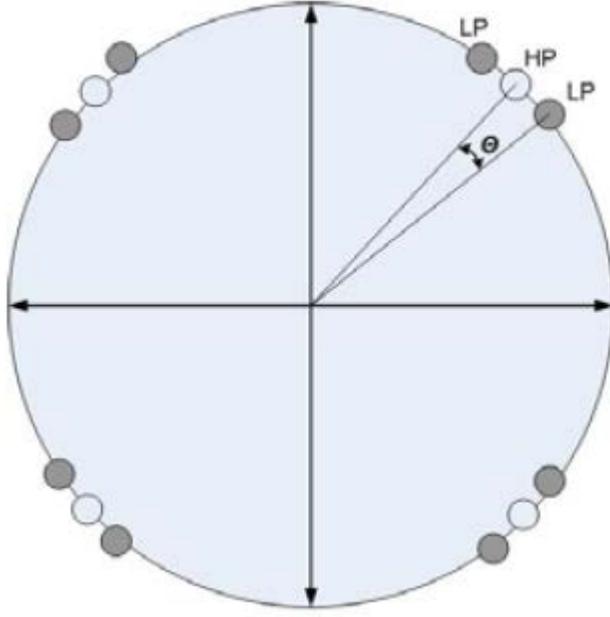


Figure 2. Depiction of hierarchical modulation of 8PSK signal on a legacy QPSK signal. From [1].

2. Layered Modulation

Layered modulation is a technique in which two satellite communication signals are transmitted on the same uplink channel forming a super-positioned signal on the downlink [1]. The benefit of this bandwidth reuse technique is that the effective spectral efficiency of a set bandwidth on a satellite transponder can be increased by either increasing receiver complexity or transmitted signal power. The increase in efficiency results mostly through modifications to the ground segment. Increases in ground equipment complexity and power will almost always be more cost effective than increasing the requirements of the satellite transponder [5]. The greatest benefit of this technique is the savings of bandwidth as seen in Figure 3.

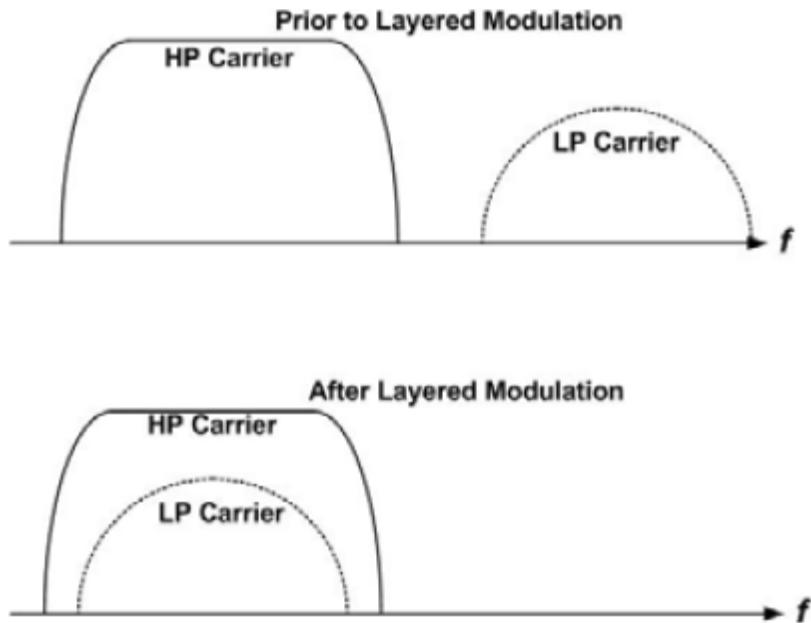


Figure 3. An example of bandwidth reuse through layered modulation. From [1].

a. Layered Demodulation

To demodulate the mixed downlink signal, digital signal processing is used to cancel one of the two signals in the receiver, resulting in recovery of the second signal. Two methods for cancelling the first signal have been identified [1]. In the first method the first signal is known *a priori* by the receiver, perhaps from a paired transmitter at the receiver's location in a two-way communications system. In the second method, the two uplink signals differ significantly in power levels resulting in a high-power (HP) signal and a low-power (LP) signal. The difference in power levels allows the HP signal to be demodulated directly by the receiver. If the LP signal desired, then after demodulating the HP signal, the receiver can re-modulate that signal to create an inverted replica to cancel the original downlinked HP signal. This action results in the LP signal which can then be demodulated directly. Both of these methods are depicted in Figure 4 and are discussed in greater detail below [1].

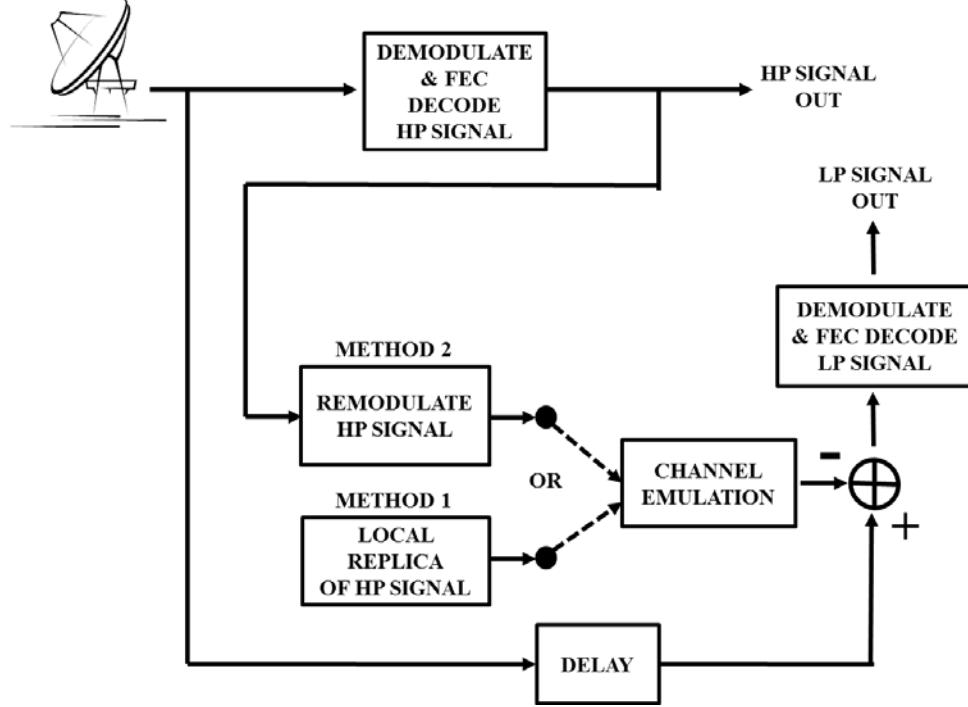


Figure 4. A model of methods to demodulate a layered modulation signal. After [1].

(1) Method One: A Priori Knowledge

This method of performing layered demodulation is by far the most popular and is employed commercially in products from both Viasat and Comtech EF Data. This method's popularity is due to multiple factors. In most fixed point-to-point communication architectures, the receiver has access to only one of the two signals. Cancellation becomes a matter of delay, scaling, and optional channel filtering. There is not a requirement for significantly higher power levels to be employed. The only additional noise in the link margin results from the performance of the signal canceller. As a result, this technique is heavily marketed by both Viasat and Comtech EF Data as allowing savings up to 50% [5]. With this technique, it is also possible to impact an entire network by upgrading only one ground station. In the common VSAT hub and spoke configuration, if the broadband hub is equipped with the ability to perform layered demodulation and increases its power level, the narrowband spokes can use the same frequencies for their return signals. The power of the return signals is maintained high enough so that the hub can demodulate the return signals after canceling its own signal

from the downlink. The power of the hub is maintained sufficiently high so that the return signals sharing the bandwidth do not interfere with the hub's outbound communications.

This method of layered demodulation is not without issues. First, there is delay in a satellite communications signal transmitted and returning in the downlink as a result of the 72,000 km roundtrip distance the signal must travel in the case of geostationary satellites. This delay requires storage of the local copy of the signal and careful calculation in order to perform the cancellation [11]. Second, this method is highly sensitive to phase and frequency error between the downlinked signal and the local replica which results in poor cancellation performance [12].

(2) Method Two: Successive Demodulation

Successive demodulation has different performance characteristics than the *a priori* method discussed previously. In successive demodulation neither signal is known *a priori* and power separation must exist between the two signals in the downlink in order to allow demodulation of the HP signal despite the interference of the LP signal(s). The HP signal is first demodulated and then subsequently re-modulated, scaled, and filtered to create the cancellation signal. Depending upon the successful demodulation of the HP signal and successful cancellation, the low power signals can then be demodulated. The recovery of the low power signal is therefore dependent upon both the demodulation of the high power signal and the successful performance of the canceller in removing the high power signal from the initially received product. In the successive demodulation method, there is a lesser requirement for longer term storage of a reference signal. The parameters of the receiver that allowed successful demodulation can be used to improve the cancellation of the HP signal. For example, the phase and carrier synchronization can assist the re-modulator in creating a better replica of the HP signal for cancellation. The successive demodulation method of layered demodulation is not employed in commercial products at this time and has been only briefly addressed in research.

C. RESEARCH ON SIGNAL CANCELLATION FOR SATELLITE FREQUENCY REUSE

Frequency reuse through layered modulation was patented by ViaSat. It is currently being marketed by ViaSat Corporation as Paired Carrier Multiple Access

(PCMA) and by Comtech EF as DoubleTalk. Even the earliest academic article on the subject refers back to ViaSat corporate references in discussions on the subject [12]. Much of the scholarly research on the subject has been devoted to improving the performance of the canceller in the first method of demodulation discussed above [11]-[15]. A preponderance of the academic research on this subject has been done by Japanese researchers from Nara Institute of Science and Technology [11]-[17]. Their research falls in two general focus areas: 1) improving the performance of signal cancellation with an available local replica of one of the signals [11], [12], [14], [15], 2) improving the BER of the recovered signal through modeling the non-linear effects of the travelling wave tube amplifier (TWTA) commonly used on satellite transponders [13], [16]. The collected work of this group suggests the possibility of generating the HP signal by demodulating and re-modulating it in the receiver [11], [13], [16]. One paper focused on the effect of symbol error in the demodulation of the HP signal on the recovery of the LP signal [17]. Highlighted in this group's research is a perceived limited applicability of using the demodulated signal to generate a reference copy, as that it is limited to the case when the two signals are power separated [11]. Since the group's research focuses on applications surrounding point to multi-point duplex communications, the reasonable conclusion is that the layered modulation receiver always will have access to one of the signals *a priori*.

D. MILITARY AND CIVIL APPLICATIONS OF METHOD TWO OF DEMODULATION

Research is scarce in the area of using a demodulated HP signal to cancel the HP signal out of the super-positioned downlink in order to recover the LP signal. Common misconceptions are that there are a limited number of applications for being able to do so, and that layered demodulation receivers always have access to one of the two uplinked signals. As a result of these misconceptions, little effort has been placed into better understanding the operations of such a receiver. A reasonable application of being able to recover both signals can be argued from many useful applications. In network monitoring, it may be useful to monitor both signals in order to detect degradations in link performance by a remote station. In military signals intelligence collection, there is

an obvious need to be able to demodulate an enemy's layered modulation signals potentially with or without access to the individual uplink signals. Another reasonable application is in networks where some of the receivers are not transmitters, such as discussed with the hierarchical modulation case. Additionally, an understanding of the performance limitations of such a system also clarifies the performance limitations experienced by communications systems that are only trying to recover the HP signal, as in the hub and spoke VSAT network topology. It is the intent of this research to study the performance limitations of this method of demodulating layered modulation signals.

E. MODELING LAYERED DEMODULATION

Most of the previously discussed studies have used computer modeling and simulations to obtain the published results. An obvious benefit of the use of computer modeling is that it is easier to replicate findings and to share the model with other researchers when there is not specific hardware involved. The scalability of a computer model is also less limited, meaning new features can be added to a proven platform. The overall research proposed herein is too large for a single master's thesis. The development of a common model as a basis for continuing research prevents the generation of additional models for each stage of the research. It is for these reasons that a brief introduction into discrete-time radio design is appropriate.

F. THE UNFORTUNATE PAIRS OF THE SET, {ANALOG, DIGITAL}

To be clear with what is meant by discrete-time radio design, a quick introduction to some terminology is helpful. In common parlance, the terms digital and analog are used to describe both signal modulation types and the manner in which the hardware to recover and process these signals are implemented. These descriptors result in the pairs: digital-digital, digital-analog, analog-digital, and analog-analog. Ambiguity results in unfortunate terms such as an analog-digital radio which intends to refer to a digital radio implementation that recovers analog signals, such as broadcast frequency modulation signals. The terms discrete-time and continuous-time are used to describe the radio implementation throughout this thesis, a distinction courtesy of Dr. Michael Rice [18].

G. THE CASE FOR DISCRETE-TIME RADIO DESIGN

The rising trend of discrete-time radio design can be credited to three major factors: digital logic, digital signal processing, and the improved design cycles of these systems. Digital logic has benefited from its consistent development following Moore's law resulting in increasing computational speed, decreased size, and competitive pricing. It is no wonder that the ubiquitous mobile cellular phone is largely implemented with digital logic [18]. The power of digital logic is harnessed for transmitter and receiver using discrete-time processing. Designs in discrete-time can be rigorously tested without hardware, which means that designers can step out of the design-implement-test-redesign-implement-retest loop. Digital designs often incorporate flexible designs, which mean that system capabilities may be modified after manufacturing to either troubleshoot issues or to introduce new features without additional manufacturing [18]. Discrete-time radio designs are the gateway characteristic which enables other technologies such as software-controlled radios, software defined radios, and cognitive radios. It is almost certain that, until there is a paradigm changing discovery in communications engineering, modern radios will continue to be designed using discrete-time processing.

H. ORGANIZATION OF THIS THESIS

This thesis is organized into six chapters. Background information that will prepare the reader for the discussion that follows is contained in Chapter II. Research into the development and use of a discrete-time receiver in investigating the performance of a successive demodulation approach for recovering both signals in layered modulation communications is outlined in Chapter III. The incremental design of a discrete-time transmitter and receiver is documented in Chapter IV. The testing of this receiver in demodulating a signal both with and without the presence of co-channel interference is discussed in Chapter V. In Chapters VI and VII, this thesis is concluded with an exploration of future research and a summary of the work completed. Appendices are included for additional detail that would otherwise detract from the flow of this document and include supplementary materials, such as the Simulink model files and associated Matlab script files.

II. BACKGROUND

Having introduced the topic of this research, some background information that lays a foundation for the design and research follows. The background material in this chapter is provided to enable the reader to better understand the research results described within this thesis.

A. THE SATELLITE COMMUNICATIONS CHANNEL

Communications between ground stations and orbiting communication relays are made through the satellite communications channel. This channel is primarily influenced by the large distances involved. The shortest path length between an equatorial fixed earth station and a geostationary communications satellite directly overhead is 35,786 kilometers, or 22,236 miles. To ensure adequate transmitter power reaches the receiver on the satellite, highly directional antennas and high power amplifiers are usually employed. The high power amplifiers by their nature are non-linear devices, but in most satellite communications applications they are operated in a linear region of operations. As a result of these two factors, the satellite communications channel is usually free of multi-path interference and is predominantly influenced by the additive white Gaussian noise (AWGN) from the thermal noise in the system [19].

B. PERFORMANCE OF BPSK AND QPSK DEMODULATORS

The derivation of the BER of a binary phase-shift keyed (BPSK) or quadrature phase shift keyed (QPSK) signal in AWGN is instructive as a means to introduce nomenclature that is used in the subsequent radio design. This is derived in many communications textbooks including [20], [21], and [22].

The signal $r(t)$ at a receiver is defined as

$$r(t) = s(t) + n(t), \quad (2-1)$$

where $s(t)$ is the attenuated transmitted signal and $n(t)$ is the noise, assumed to be AWGN with a power spectral density (PSD)

$$S_{nn}(f) = N_o / 2. \quad (2-2)$$

At the input to the receiver, the attenuated transmitted signal is

$$s(t) = \sqrt{2}A \sum_{m=-\infty}^{\infty} b_m p_T(t - mT) \cos(2\pi f_c t), \quad (2-3)$$

where the sinusoidal signal of root mean squared amplitude A and with a carrier frequency f_c is mixed with a non-return to zero (NRZ) data signal. The NRZ signal is expressed as a sequence of bits b_m expressed as antipodal values such that $b_m \in \{-1, 1\}$, and $p_T(t)$ is defined as

$$p_T(t) = \begin{cases} 1 & \text{if } 0 \leq t < T \\ 0 & \text{otherwise} \end{cases} \quad (2-4)$$

where the pulse duration T is related to the bit rate $R_b = 1/T$. The energy of a bit is [20]

$$E_b = A^2 T. \quad (2-5)$$

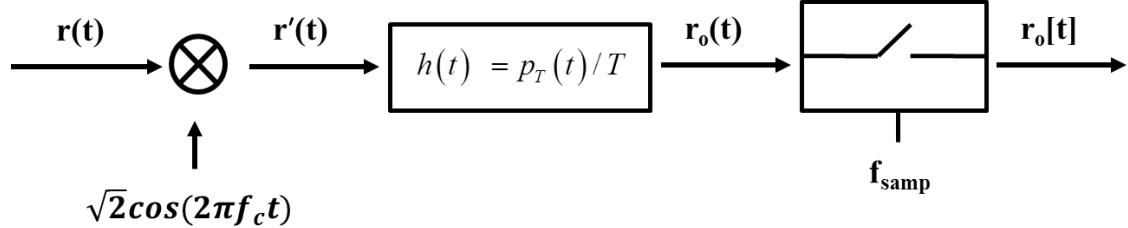


Figure 5. Depiction of a segment of BPSK receiver.

Figure 5 is a diagram of the signal flow through a BPSK receiver. The down-converted received signal is annotated $r'(t)$ and is the input to the matched filter, which has impulse response $h(t)$. The output of the matched filter is annotated $r_o(t)$ which is then sampled at the sampling rate f_{SAMP} , which is ideally equal to $1/T$, resulting in the discrete-time signal $r_o(t)$. From Figure 5 and Equations (2-1) and (2-3), it is easily shown that

$$r'(t) = A \sum_{m=-\infty}^{\infty} b_m p_T(t - mT) + A \sum_{m=-\infty}^{\infty} b_m p_T(t - mT) \cos(4\pi f_c t) + \sqrt{2}n(t) \cos(2\pi f_c t). \quad (2-6)$$

The output $r_o(t)$ of the matched filter is the result of the convolution of $r'(t)$ with $h(t)$.

The second term in $r_o(t)$ drops out as result of it being a double frequency term which is filtered out by the matched filter resulting in

$$r_o(t) = r'(t) * h(t), \quad (2-7)$$

$$r_o(t) = A \sum_{m=-\infty}^{\infty} b_m p_T(t - mT) * \frac{1}{T} p_T(t) + \sqrt{2} n(t) \cos(2\pi f_c t) * \frac{1}{T} p_T(t). \quad (2-8)$$

We define $n_o(t)$ as the second term on the right hand side of (2-8). The mean value of $n_o(t)$ is zero because the mean value of $n(t)$ is zero. The variance of $n_o(t)$ follows from (2-8) and (2-2) as

$$\overline{n_o^2(t)} = \sigma^2 = \frac{N_o}{2T}. \quad (2-9)$$

In the end, we are left with an expression for the output of the matched filter

$$r_o(t) = A \sum_{m=-\infty}^{\infty} b_m \Lambda(t - (m+1)T) + n_o(t). \quad (2-10)$$

where $n_o(t)$ is a colored Gaussian random signal with variance, or noise power, of $N_o / 2T$. $\Lambda(t)$ is defined as

$$\Lambda(t) = \begin{cases} \frac{t}{T} + 1 & -T \leq t \leq 0 \\ -\frac{t}{T} + 1 & 0 < t \leq T \\ 0 & otherwise \end{cases} \quad (2-11)$$

As a result, the sampled signal $r_o[kT]$ is equal to

$$r_o(kT) = A \sum_{m=-\infty}^{\infty} b_m \Lambda(kT - (m+1)T) + n_o(kT), \quad (2-12)$$

$$r_o(kT) = A b_{k-1} + n_o(kT) = \pm A + n_o(kT). \quad (2-13)$$

With Equation (2-13) the bit error ratio of the BPSK signal is given by

$$BER = \Pr\{r_o(kT) < 0 \mid b_{k-1} = 1\}, \quad (2-14)$$

which can have Equation (2-13) substituted in and normalized into,

$$BER = \Pr\left\{-\frac{n_o(kT)}{\sqrt{\sigma^2}} > \frac{A}{\sigma}\right\} = Q\left(\frac{A\sqrt{2T}}{\sqrt{N_o}}\right) = Q\left(\sqrt{\frac{2E_b}{N_o}}\right), \quad (2-15)$$

where the final expression in Equation (2-15) is the familiar result for the BER of a BPSK signal.

A QPSK signal $s_{QPSK}(t)$ can be thought of simply as two orthogonally multiplexed BPSK signals

$$s_{QPSK}(t) = \sqrt{2}A \sum_{m=-\infty}^{\infty} b_m p_T(t - mT_b) \cos(2\pi f_c T) - \sqrt{2}A \sum_{m=-\infty}^{\infty} c_m p_T(t - mT_b) \sin(2\pi f_c T) \quad (2-16)$$

where c_m is a bit sequence similar to b_m . The resulting QPSK signal has twice the power and twice the bit rate of a single BPSK signal. Therefore, this QPSK signal has the same energy per bit $E_{b,QPSK} = 2A^2(T_b / 2) = A^2T_b$ as a BPSK signal, where each orthogonal QPSK channel has the same bit duration as the BPSK signal. Since the BER performance of each orthogonal QPSK channel is $Q\left(\sqrt{2E_b / N_o}\right)$, the BER performance of the optimum QPSK receiver is also $Q\left(\sqrt{2E_b / N_o}\right)$.

C. IMPACT OF PHASE/FREQUENCY ERROR ON A QPSK RECEIVER

QPSK is a coherent form of communications. That is, the transmitter and the receiver need to be synchronized in regards to carrier frequency and phase as well as symbol timing for optimum detection in the presence of noise. In order to achieve this, real-world receivers employ synchronization circuits in an attempt to closely match the oscillator and clock in the transmitter. The importance of phase and frequency synchronization circuits can be seen in an evaluation of the impact of phase error θ_e on a

QPSK radio receiver. The following explanation parallels a more detailed derivation in [18]. The phase error is defined as the phase of the communications signal at the receiver minus the phase of the local oscillator in the receiver.

If we define $r'(t)$ as the received rotated QPSK signal at the receiver which is composed of an in-phase antipodal pulse train $I(t)$ and a quadrature antipodal pulse train $Q(t)$, then we can express $r'(t)$ as

$$r'(t) = I(t)\sqrt{2} \cos(2\pi f_c t + \theta_e) - Q(t)\sqrt{2} \sin(2\pi f_c t + \theta_e). \quad (2-17)$$

Using a trigonometric identity, we can recast Equation (2-17) into

$$r'(t) = I_r(t)\sqrt{2} \cos(2\pi f_c t) - Q_r(t)\sqrt{2} \sin(2\pi f_c t), \quad (2-18)$$

where

$$\begin{aligned} I_r(t) &= [I(t) \cos(\theta_e) - Q(t) \sin(\theta_e)] \\ Q_r(t) &= [I(t) \sin(\theta_e) + Q(t) \cos(\theta_e)]. \end{aligned} \quad (2-19)$$

Equations (2-19) provide insight into the impact of phase error on the received QPSK signal. If the phase error is zero, we can see that the term from the other channel drops out of each of the equations. If there is phase error, then the desired channel component is attenuated, and the other channel component is introduced. If we define the desired, unrotated signal vector $\vec{r}(t)$ to be

$$\vec{r}(t) = \begin{bmatrix} I(t) \\ Q(t) \end{bmatrix}, \quad (2-20)$$

then Equation (2-19) can be transferred into matrix form, showing that the phase error creates a rotation matrix that acts upon the unrotated signal vector. The result is that the rotated signal vector $\vec{r}'(t)$ is given by

$$\vec{r}'(t) = \begin{bmatrix} I_r(t) \\ Q_r(t) \end{bmatrix} = \begin{bmatrix} \cos(\theta_e) & -\sin(\theta_e) \\ \sin(\theta_e) & \cos(\theta_e) \end{bmatrix} \vec{r}(t). \quad (2-21)$$

The impact of the rotation on the BER can be seen simply from the fact that the desired channel's signal is attenuated by the cosine of the phase error. This results in the frequently derived BER for QPSK with a phase error [20]

$$BER = Q\left(\sqrt{\frac{2E_b}{N_o}} \cos(\theta_e)\right). \quad (2-22)$$

If we were to look at the impact of the rotation on the noise signal in the receiver, we would see that the noise and noise power are not impacted by the rotation. As mentioned before, the noise in the in-phase and quadrature channels are independent and identically distributed (IID) with the same noise power and form a joint probability function which is circularly symmetric and, therefore, not impacted by rotation. Any rotation of the final constellation simply reduces the Euclidean distance between the received signal and an adjacent decision region, thereby increasing bit error.

A simple phase error between the transmitter and the receiver can be modeled as a finite step error if the steady-state phase error is a constant. Since frequency is the derivative of instantaneous phase, a step in frequency can be seen as a ramp error in phase, which is a function of time. These two concepts become important in the following discussion on phase-lock loops. Before discussing phase-lock loops, a review of the impact of symbol timing errors is appropriate.

D. IMPACT OF TIMING ERROR ON A QPSK RADIO RECEIVER

To discuss timing error, it is useful to review the output of the two common signal detectors used in digital radios: the correlator and the matched filter. In Figure 6, the important take away regarding these two detectors is that, at the correct sampling instant, the outputs of both detectors are identical.

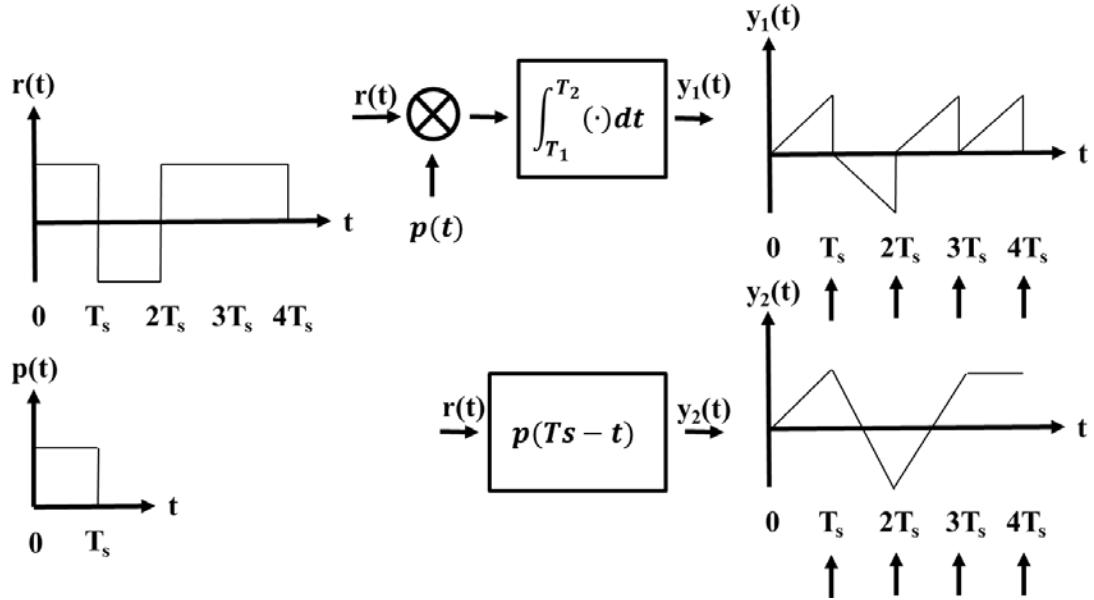


Figure 6. Illustration of the outputs of a correlator and a matched filter at sampling time T_s . After [18].

If the receiver samples the output of either of these detectors earlier or later than the correct sampling instant, then the result is an attenuated version of the optimum value. This attenuation in the output power becomes important when noise is also introduced to the detectors. If the signal value is attenuated, the noise has an increased probability of generating an error when the receiver makes its decision. The eye diagram is a common diagnostic tool to visualize the detector output at the sampling time. Figure 7 is an eye diagram from the in-phase detector on a discrete time QPSK receiver. The detector samples at the even seconds, which does not correspond to the widest possible opening in the eye and, therefore, are not the optimal times for sampling to reduce the impact of noise. The ideal sampling times are approximately 125 msec after the even seconds, a fact indicated by the location of the zero crossings.

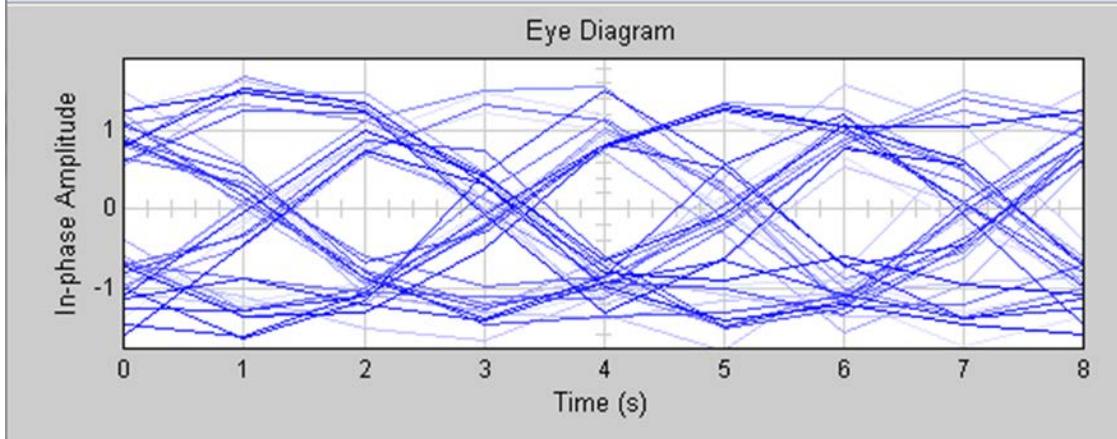


Figure 7. The eye diagram of the matched filter output of discrete time QPSK receiver.

Both phase/frequency error and timing error result in a reduction of the signal amplitude at the detector at the sampling time, essentially resulting in a decrease of the signal to noise ratio (SNR) which determines the BER of the receiver. In other words, to increase performance, the receiver must employ a mechanism to determine the phase and timing errors and to correct them. In order to do so, the synchronization circuits use phase-lock loops (PLLs).

E. PHASE-LOCK LOOPS

Phase-lock loops are used in both carrier phase/frequency synchronization circuits and in timing synchronization circuits. PLLs are simply control algorithms which measure error and then appropriately apply a control signal in order to drive the error to the desired value, in this case zero. A PLL consists of three elements: a phase detector, a loop filter and a controllable oscillator [23]. To generalize the use of PLLs to timing synchronization circuits, the three elements can be considered as a timing error detector, a loop filter, and a controller as depicted in Figure 8. The error detector produces an output proportional to the instantaneous timing error. The loop filter implements a control algorithm designed to mitigate the impact of noise on the PLL. In general it can be considered to be performing an averaging operation, through which the actual mean error can be separated from instantaneous error caused by noise. The controller is the means by which the error is corrected.

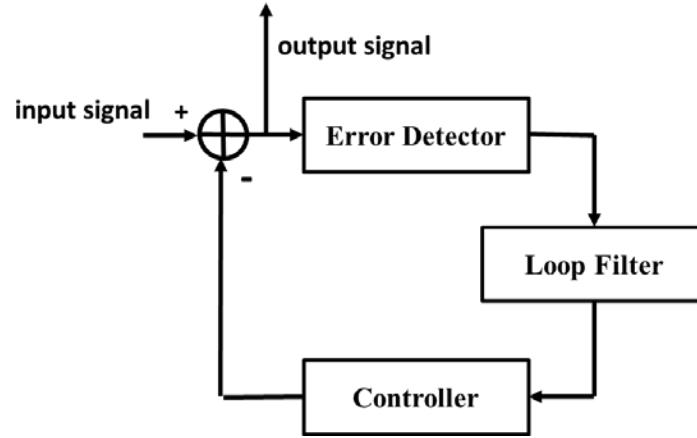


Figure 8. The diagram of a phase lock loop with alternate nomenclature.

In the end, the PLL is a control loop. As such, the type of loop equation, or the transfer function used, influences the type of errors that the loop can correct. In general, a second-order loop has the ability to drive step errors and ramp errors to zero [23]. In the case of the carrier phase/frequency synchronization circuit, a properly tuned second-order PLL can correct both constant phase error, which is a step phase error, and a constant frequency error i.e., a ramp phase error. A popular loop filter, which is employed in the receiver designed in this research project, is the proportional-plus-integrator filter, which is written as $H(s)=K_1+K_2/s$ in the Laplace domain.

Given the above background information, we are prepared to continue with the research methodology that is employed.

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III. RESEARCH METHODOLOGY

The goal of this work is to study the performance of successive demodulation in recovering information from power-separated, layered modulation signals by simulation using a discrete-time QPSK receiver model. A four phased approach was initially proposed with the following phases: Discrete-Time Radio Design, Single Signal Receiver Performance, Layered Demodulation Receiver Design, and Layered Demodulation Receiver Performance Testing. During the course of this research Phase One was completed as well as a majority of Phase Two. The proposed approach for Phases Three and Four are discussed further in Chapter VI on future work.

A. PHASE ONE: DISCRETE-TIME RADIO DESIGN

The goal of the first phase of the research is to design and model a realistic discrete-time QPSK radio receiver for use in subsequent research. In order to be realistic, the designed radio must not have access to either the transmitter's up-conversion oscillator or symbol timing clock and must be able to mitigate errors in phase/frequency and symbol timing introduced by the channel. This requirement results in the inclusion of both a carrier phase/frequency synchronization circuit and a timing synchronization circuit in the final design. Any assumptions made in the design of the system, such as a requirement for training sequences, are discussed in the documentation of the design. As part of the design, incremental testing was conducted to ease troubleshooting issues with the design. The end product of this phase is the functioning model of a QPSK receiver which is ready to enter performance evaluations.

B. PHASE TWO: SINGLE RECEIVER PERFORMANCE

In the second phase of the research, the radio designed in phase one was tested to identify its BER performance against the theoretical performance of an ideal QPSK radio receiver. Any notable discrepancies between actual and theoretical performance are discussed. Upon satisfactory performance in this testing, the receiver was used to quantify the impact on the high powered signal's BER in the receiver when linearly superimposed with a LP signal of various power ratios. The end state of this phase is a

suitable radio receiver which will be a building block in the design of a successive demodulator.

IV. DISCRETE-TIME RADIO DESIGN

In this phase of the research, the goal is to design a realistic discrete-time QPSK radio receiver which can be used as a building block for subsequent research. The design of the radio is documented incrementally in order to facilitate replication of the design. Further details are located in the appendices and supplemental materials. Any additional discrete-time circuits designed to test the receiver, such as the transmitters used to test the designs, are also explained.

A. COHERENT ONE SAMPLE PER SYMBOL BPSK RADIO RECEIVER

As an exercise in the design environment, Simulink, a baseband BPSK radio transmitter and receiver design found on the World Wide Web was employed in this study [24]. The design is implemented entirely with existing Simulink blocks which assisted in gaining familiarity with the existing object libraries. The overall model is displayed in Figure 9. The design uses a **random integer generator** to generate a binary sequence. The binary sequence is connected to a **Simulink baseband BPSK modulator** which outputs a complex representation of the BPSK signal to the channel. The channel is modeled with another Simulink object, the **AWGN channel**. The **AWGN channel** allows the SNR of the output to be set directly in the parameters settings. The output of the **AWGN channel** is a complex BPSK signal with AWGN noise, which accurately impacts not only the amplitude of the BPSK signal but also the phase. The demodulator is another Simulink system block, **BPSK demodulator baseband**. This block receives the complex BPSK signal with noise and demodulates it back to a binary sequence. This system incorporates scatter plots of the signal at the output of the transmitter and input of the receiver, which allow for easy visualization of the impact of noise on the system. A highlight of the system is the use of a Simulink **error rate calculation** block. The **error rate calculation** block uses the input bit stream and the output bit stream providing real-time BER analysis into a display block.

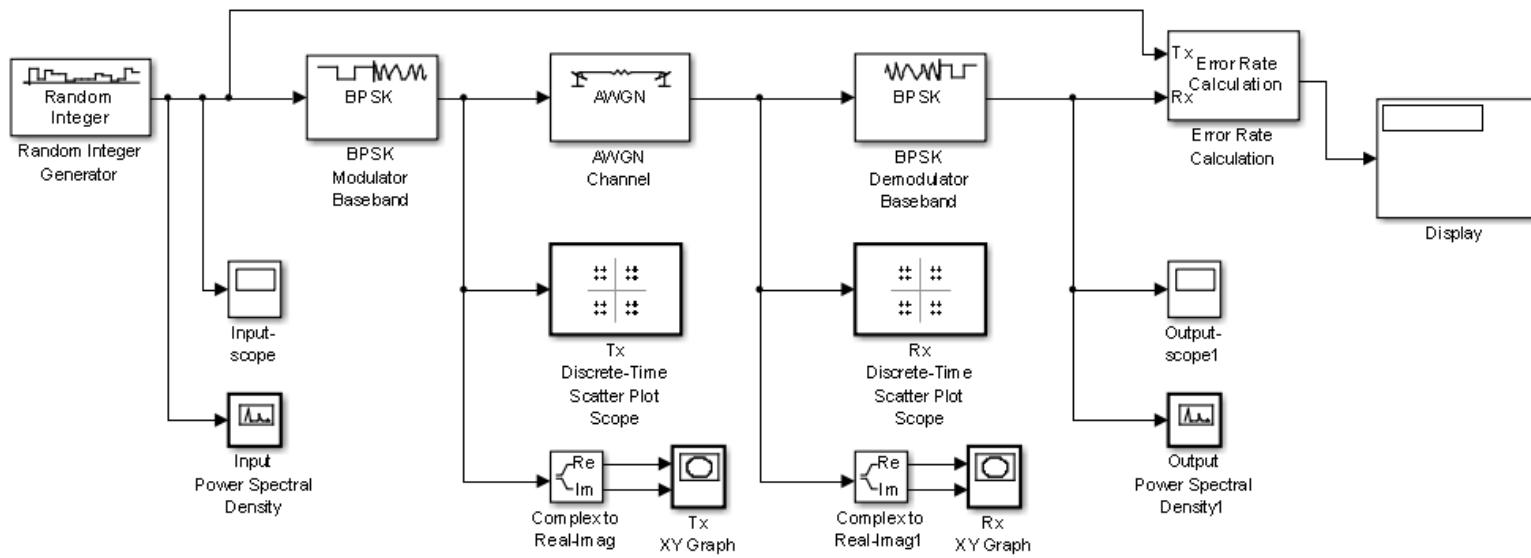


Figure 9. A baseband BPSK transmitter and receiver. After [24].

This system has several limitations, primarily because it is only a model of a communication system. This system is at baseband with no up-conversion before entering the channel at the transmitter and no down-conversion when exiting the channel at the receiver. As a result, neither the transmitter nor receiver has an oscillator to be synchronized. Since the symbols are only generated and transmitted at one sample per symbol at baseband, the transmitter and receiver are automatically synchronized in symbol timing. Symbol timing error can only be introduced if the receiver can possibly sample at the wrong time. This model is indeed a discrete-time transmitter and receiver but far from being a realistic implementation in that propagation does not occur at baseband with a reasonably sized antenna.

B. COHERENT MULTI-SAMPLE PER SYMBOL BPSK RADIO RECEIVER

To improve upon the radio in the previous section, the follow-up design must incorporate the transmitted signal passing through the channel as a bandpass signal, even if only in discrete-time. Additionally, the symbol should be a multiple sample per symbol shaped pulse before being up-converted for transmission. The initial model was abandoned for two reasons: 1) since the goal was discrete-time implementation, any object used in the transmitter, and especially the receiver, must be implementable in digital logic, and 2) the Simulink blocks used only complex single sample-per-symbol representations for signaling. Complex representations can be implemented into a discrete-time system with two wires, one carrying the magnitude and the other carrying the phase. This researcher elected to use a conventional representation in designing the discrete-time radio receiver rather than a complex representation in keeping with the goals of the research.

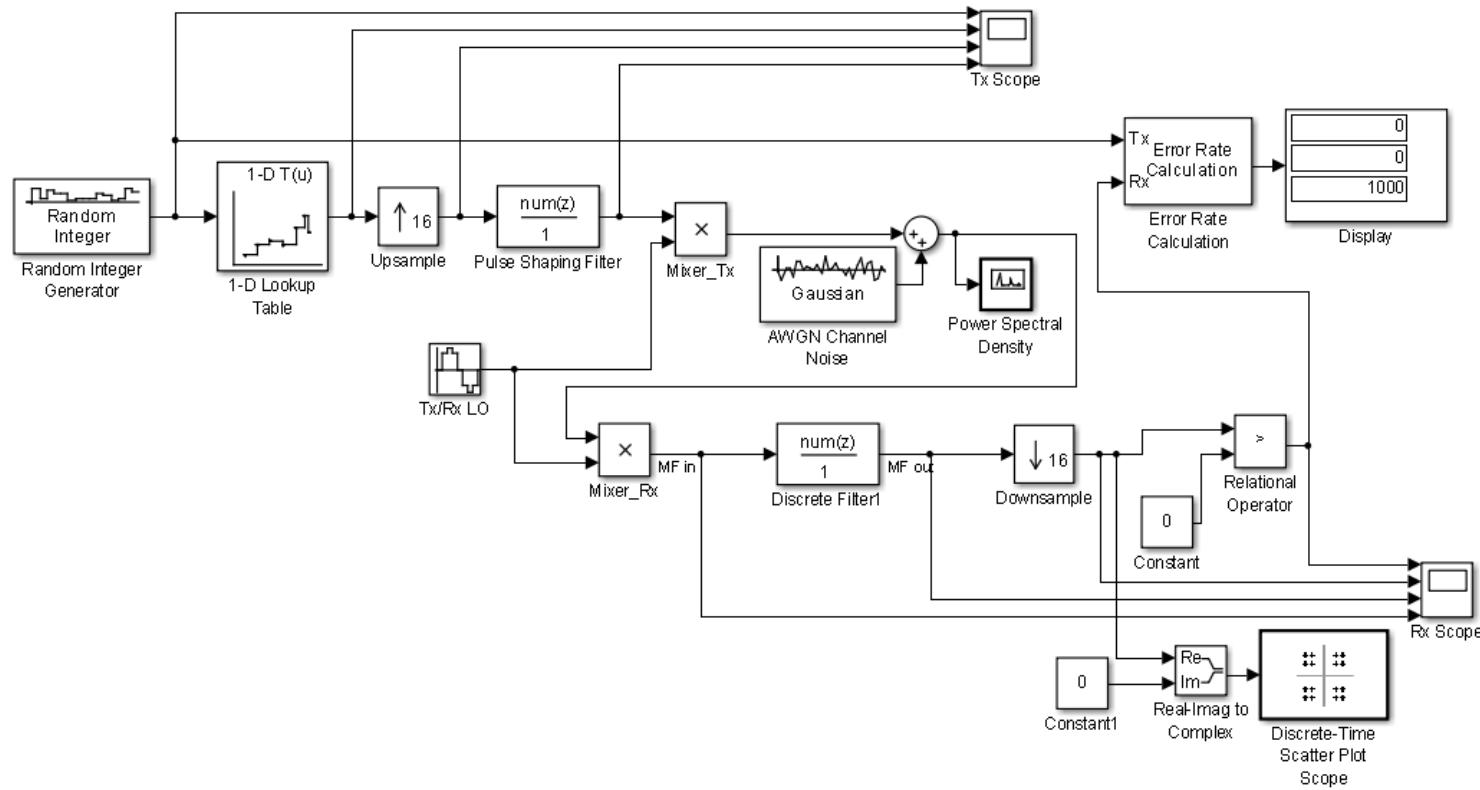


Figure 10. A Coherent multi-sample-per-symbol BPSK communications system.

The implementation of the first multi-sample per symbol radio design is shown in Figure 10. The binary sequence is still generated by a random integer generator, which outputs the ordered sequence b_n that consists of elements of the set $\{0,1\}$ at the designated sample rate. This binary sequence is mapped to the set $\{1,-1\}$ which could also be accomplished by the function $f[n]=2b_n-1$. The output of this mapping is then up-sampled by 16 to create an impulse stream by inserting 15 zeros after every pulse. The pulse shaping is applied by a pulse shaping filter. In this receiver, rectangular NRZ pulse shaping was desired, as well as unit bit energy, so the coefficients of the numerator of the discrete transfer function used was

$$H(z) = \frac{1}{4} \sum_{i=0}^{15} z^{-i}. \quad (4-1)$$

The evolution of the data stream into polar pulses is shown in Figure 11. While the second and fourth plots in the figure look similar, the fourth plot has 16 samples per symbol as opposed to one sample per symbol as in the second plot. Additionally, the fourth plot is scaled for unit energy for each symbol/bit.

The next step is the up-conversion of the NRZ signal into a bandpass signal. The conversion is accomplished simply through multiplication of the NRZ signal with a scaled cosine at the carrier frequency. The scaling of the cosine by the square root of two results in the generated symbol having unit energy which simplifies things when noise is added to the channel. If this model was actually implemented in practice, a direct digital synthesizer (DDS) would be employed to convert the signal to a continuous-time signal. Many of these devices have digital words which establish the amplitude of the output signal and words which allow for selection of the phase of several coherently generated sinusoids, allowing easy conversion to continuous time.

In the channel, the addition of AWGN is accomplished by the use of a Simulink object, **AWGN channel noise**, which is added to the transmitted signal. The power of the AWGN noise is controlled directly by a block parameter, the variance of the noise. Since the transmitted signal has unit bit energy with known duration T , it is relatively

straightforward to configure the SNR of the signal at the receiver, recognizing that the variance of the noise is $N_o / 2T$ from Equation (2-9).

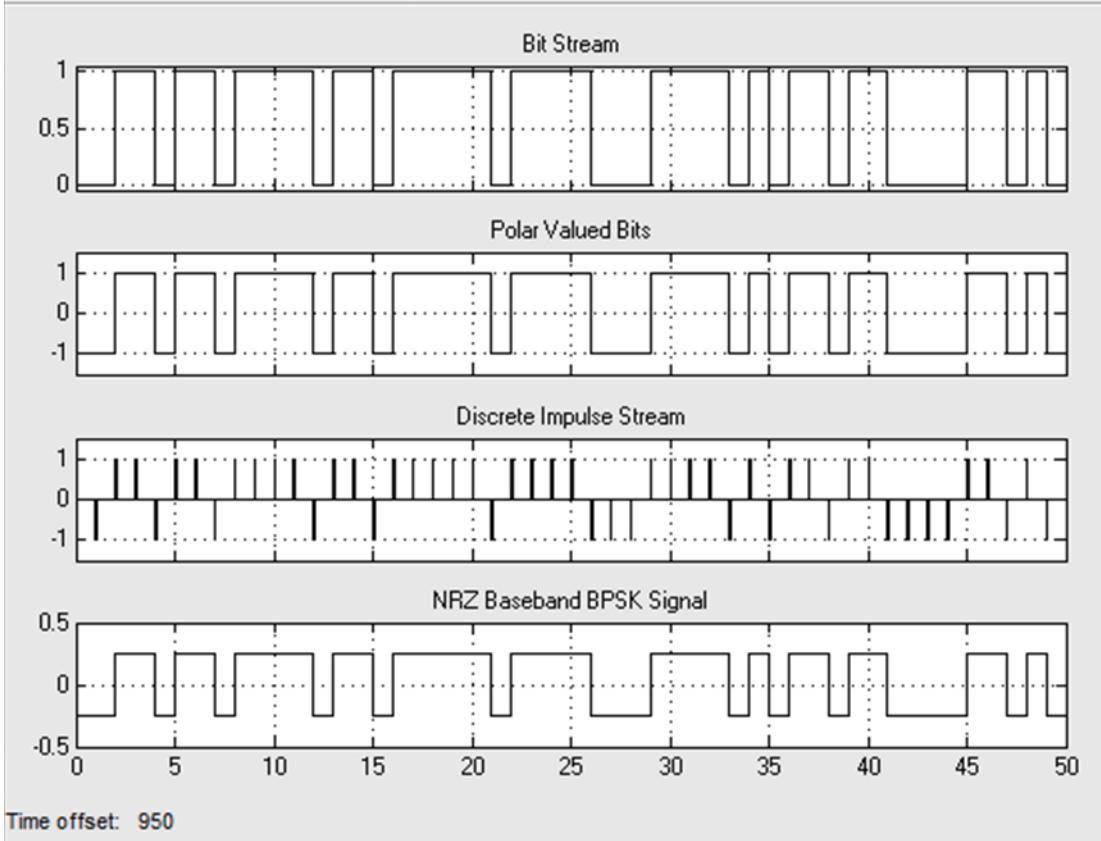


Figure 11. The evolution of a bit sequence into a NRZ baseband BPSK signal.

Analysis of the receiver quickly reveals that the design has obviously coherent oscillators in the transmitter and receiver. In fact, they are the very same oscillator. If this model of the receiver was implemented in practice there would be a design decision on where to convert from continuous-time to discrete-time with an analog-to-digital converter and in which domain down-conversion occurs. Regardless, the baseband signal is convolved with a matched filter (MF) using the same filter coefficients as the pulse-shaping filter. The input and output of the receiver's MF are shown, respectively, in the fourth and third scope outputs of Figure 12. The output of the MF is down-sampled back to a single sample per symbol in order to determine the bit value by a threshold detector. The outputs of the down sampler and the comparator are shown in scopes 2 and 1 of Figure 12.

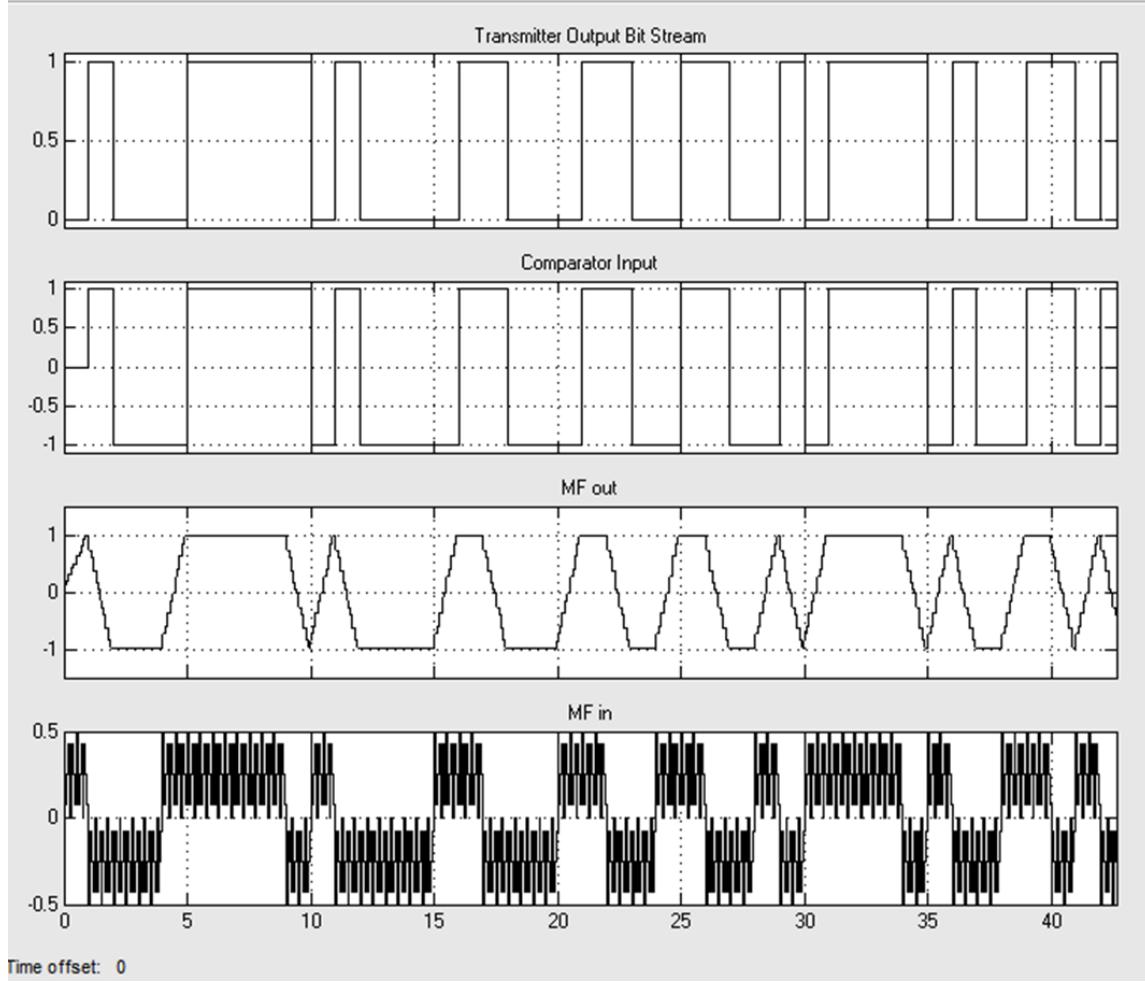


Figure 12. Transformation of received signal back into bit stream.

This radio design is much closer to the goal of a realistic receiver. Even though it shares an oscillator with the transmitter, it realistically generates a bandpass signal and even demonstrates some of the impact of symbol timing error. The timing error was subsequently removed by adjusting the sample offset parameter in the down-sampling block. An important lesson learned during the design of this radio is that to avoid the tedious nature of having to open a multitude of object parameter dialogs, symbolic values can be placed in many of the parameters such as noise power that require frequent adjustment. A MATLAB script can be used to maintain the desired settings. The settings in the MATLAB script can be quickly applied by running the script, saving the operator from having to open many different dialogues. Additionally, individual object parameter dialogs do not need to be opened to find mis-typed parameter values when

troubleshooting. The next step in design was to include pairing two BPSK transmitters and receivers into a QPSK system.

C. COHERENT MULTI-SAMPLE PER SYMBOL QPSK RADIO RECEIVER

The design of the QPSK transmitter followed rather quickly from the coherent multi-sample-per-symbol BPSK communications iteration. The complete design of the QPSK transmitter circuit is shown in Figure 13. The input signal designated $m(t)$ is the same randomly generated integer used previously. The serial-to-parallel converter was implemented using down-samplers and unit delays. Since down-conversion by two requires discarding every other sequence value, the bit stream to the I channel was down-converted first to discard the Q-channel bits and then delayed to match the timing of the Q-channel bits. The Q-channel bits were delayed first and then down-sampled to discard all of the I-channel sequence values. Thus, the serial input with a bit period of T_b was converted to a two element parallel bit stream with period $2T_b$. The rest of the transmitter design follows from the previous design iteration. Of note are the inclusions of separate oscillators for the in-phase and quadrature channels rather than using a phase delay from a common oscillator for the second channel. This design decision allows for analysis of the effects of amplitude and phase mismatches introduced by the slight differences between the balanced modulators in the I and Q channels [25].

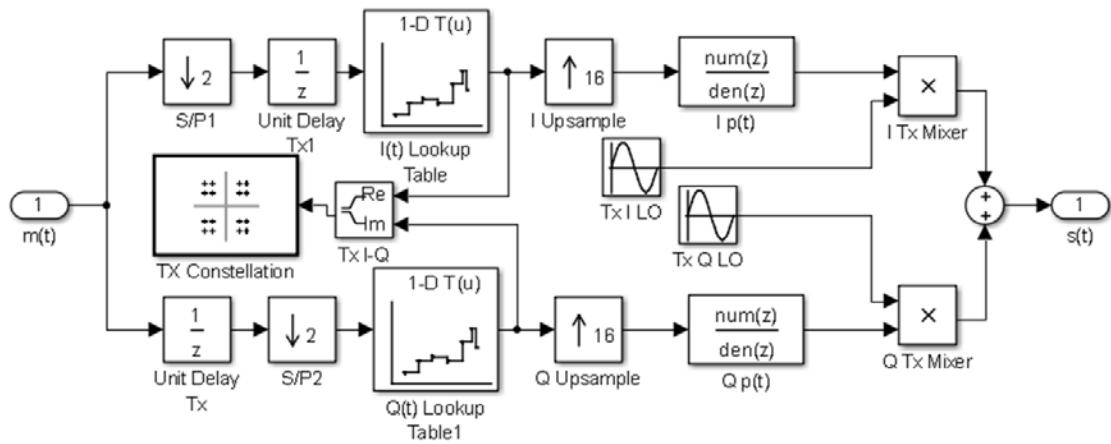


Figure 13. QPSK discrete-time transmitter subsystem.

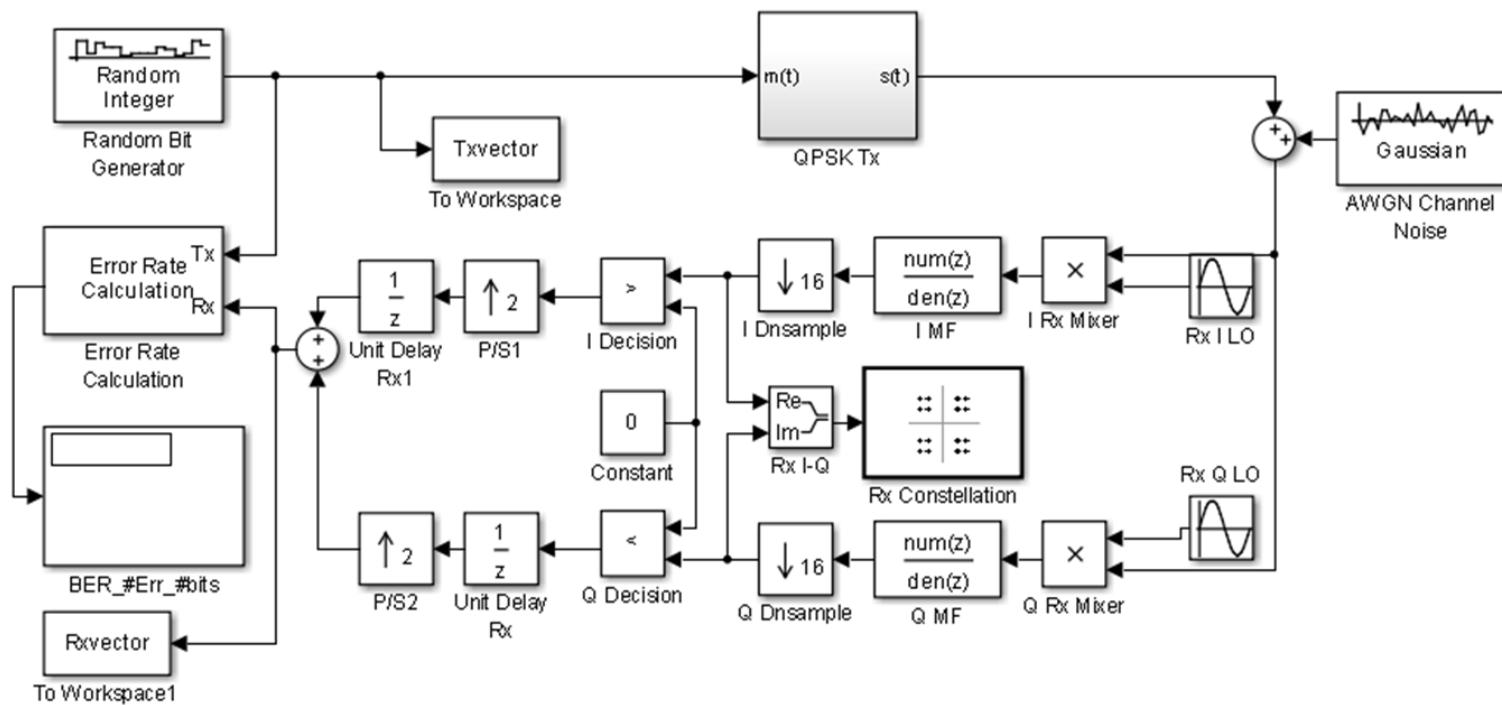


Figure 14. Discrete-time QPSK transmitter and receiver circuit.

The design of the receiver displayed in Figure 14 is virtually analogous to the transmitter. Also of note is the use of separate oscillators in the receiver circuit. The parallel-to-serial conversion was accomplished using unit delays and up-sampling, inserting zero values into the sequences. Similarly, $2T_b$ is the bit duration of each of the parallel bit streams, and the resulting composite bit stream has a bit duration of T_b . This circuit is ideal for investigation of the impact of phase error on the BER of a QPSK receiver in that the phases of the transmit oscillators and receive oscillators can be mismatched to produce the desired phase error.

D. QPSK PHASE/FREQUENCY SYNCHRONIZATION CIRCUIT

In Chapter II, the impact of phase error on the received signal was discussed. Phase error was portrayed as a parameter of the rotation matrix that acts upon the received signal vector. Before a phase/frequency error can be corrected, it must be detected. Once a phase/frequency error is detected, there are several opportunities and methods to correct the error. A phase-error detector operates in the presence of noise; therefore, a filter is necessary to mitigate the impact of noise on the detector. These elements-- a phase-error detector, a loop filter and a controller-- create a phase-lock loop as described in Chapter II. The key elements of the phase/frequency synchronization circuit are displayed in Figure 15.

1. Phase Error Detector

Computing phase error can be accomplished by comparing the values of the MF output at the sampling time to the received signal vector that was selected by the detector. In Figure 16, the phase of the received signal vector θ_r is shown in relation to the phase of the decision signal vector θ_d . The phase error displayed in this case is

$$\theta_e = \theta_r - \theta_d . \quad (4-2)$$

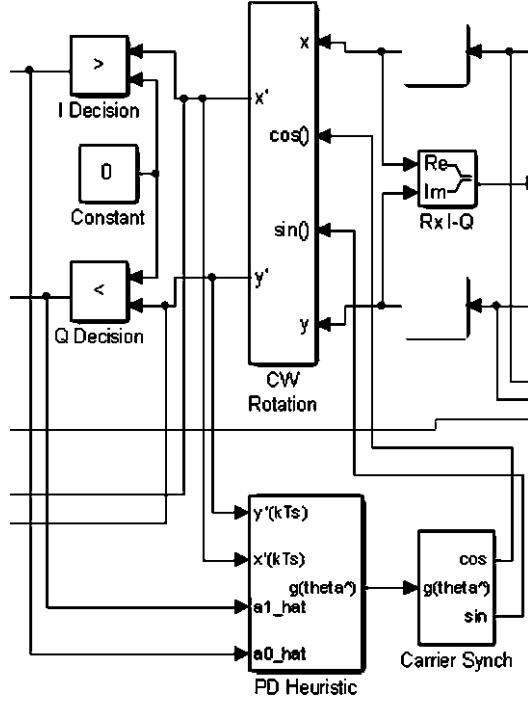


Figure 15. Elements of phase/frequency synchronization circuit.

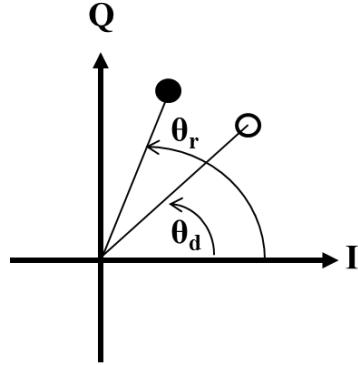


Figure 16. The phase angles of received signal and decision vectors. After [18].

The values of these angles can be calculated in a straightforward manner using values that we have access to in the circuit. Using the same notation matching the labels in the synchronization circuit, we see that the value of the in-phase component of the received signal vector at the MF output is $x'(kT_s)$ and the corresponding quadrature component of the received signal vector is $y'(kT_s)$. The in-phase component of the decision signal

vector is $\hat{a}_0(kT_s)$, and the corresponding quadrature component of the received signal vector is $\hat{a}_1(kT_s)$. Using trigonometry, we can calculate the angle of the vectors from the inverse tangent of the quadrature component divided by the in-phase component. It follows that the phase error can be calculated from

$$\theta_e = \tan^{-1} \left\{ \frac{y'(kT_s)}{x'(kT_s)} \right\} - \tan^{-1} \left\{ \frac{\hat{a}_1(k)}{\hat{a}_0(k)} \right\}. \quad (4-3)$$

The connections that pass these values to the phase detector (PD) can be seen in Figure 15. Figure 17 contains an implementation of Equation (4-3) with several notable adaptations. The **division** block in Simulink does not allow division by zero. In order to avoid this error, a simple block was developed to replace zero denominators with the MATLAB epsilon constant (the next smallest value of the given floating point precision). Also, the decision vector connections pass values that are in $\{0,1\}$ binary format. To convert them back to the range $\{-1,1\}$, the value must be multiplied by two and subtracted by one. This operation also occurs in an **interpreted MATLAB function** block.

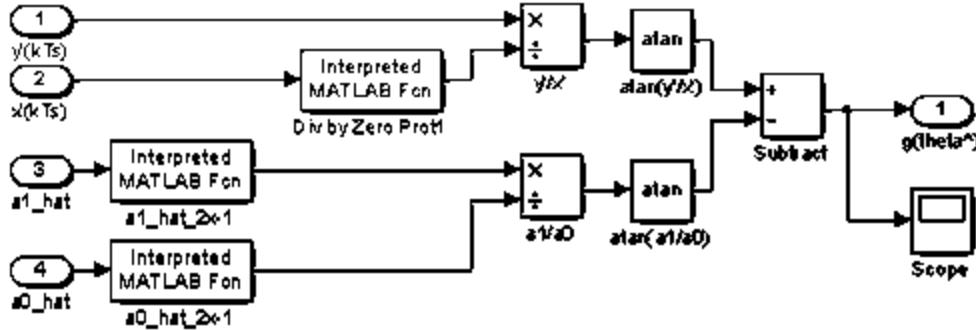


Figure 17. Phase detector sub-circuit.

2. Signal Rotator

The next element of the phase/frequency synchronization circuit is the detected phase error correction. There are two methods to correct the phase error in the receiver [18]. In the first method, the phase of the oscillator is directly adjusted by a

voltage control signal from the PLL loop filter. In the second method, the outputs of the MF are rotated in the signal space. A disadvantage of the first method is that the discrete-time oscillator in the receiver operates at a different sampling rate than the error detector, which requires signals connecting them to be converted to the appropriate sampling rate. In the second method, the entire synchronization circuit can be operated at the same sample rate. Returning to Equation (2-21), we see that if a phase error causes a rotation of the received signal space, it is necessary to rotate the signal space in the opposite direction to correct the error. Reversing the direction of the rotation matrix results by substituting $-\theta_e$ into the rotation matrix for θ_e , resulting in the counter-rotation matrix

$$\begin{bmatrix} \cos(\theta_e) & \sin(\theta_e) \\ -\sin(\theta_e) & \cos(\theta_e) \end{bmatrix}. \quad (4-4)$$

The de-rotated signal space projection is, therefore, provided by [18]

$$\begin{bmatrix} x'(kT_s) \\ y'(kT_s) \end{bmatrix} = \begin{bmatrix} \cos(\theta_e) & \sin(\theta_e) \\ -\sin(\theta_e) & \cos(\theta_e) \end{bmatrix} \begin{bmatrix} x(kT_s) \\ y(kT_s) \end{bmatrix}. \quad (4-5)$$

The values of $\cos(\theta_e)$ and $\sin(\theta_e)$ are generated by the DDS that follows the loop filter. The instantiation of the clockwise rotation block used in the radio receiver is shown in Figure 18. The operation is a direct implementation of Equation (4-5) in the Simulink environment.

1. Carrier PLL Loop Filter

The final element of the phase/frequency synchronization circuit is the loop filter sub-circuit labeled as the **carrier synch** block. The implementation of the loop filter circuit depicted in Figure 19 contains two major items: the discrete-time loop filter and the DDS. The discrete-time loop filter's transfer function is simply the second-order proportional plus integrator transfer function described in Chapter II. The derivation of the constants K_1 and K_2 used to implement this filter is described in Appendix A along with a simple explanation of the key performance parameters of the filter ζ and $B_n T$ (A lengthy description of this subject can be found in [18]).

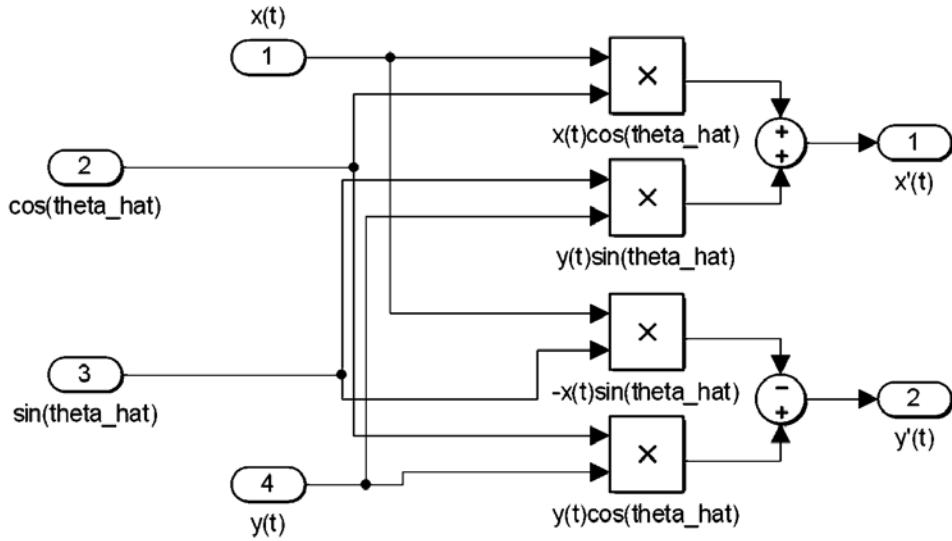


Figure 18. The implementation of a clockwise rotator for phase error correction.

Two additional constants result from the inherent gains of both the error detector K_p and the DDS K_o . The DDS was produced from an example from the World Wide Web that can no longer be located but can be replaced by any number of similar blocks. The step function is multiplied by the incoming phase error signal simply to zero out initial erroneous phase error readings before the receiver starts processing actual data. Without this step function, the carrier phase and synchronization circuit would occasionally lock into an ambiguous phase even when little or no phase error was present.

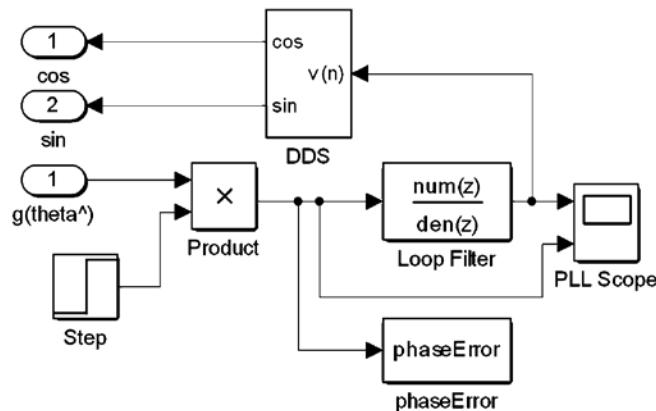


Figure 19. Loop filter and DDS of phase/frequency synchronization circuit.

An important facet of the operation of the heuristic phase detector described above is that it is decision directed. As a result, erroneous decisions can cause the phase to be locked into an erroneous value that is 90, 180, or 270 degrees from the actual phase. A quick analysis of the impact on the detected bits in the rotated constellation results in an automatic 50% BER for ± 90 degree rotations and a 100% BER for 180 degree rotation. In practice, this phase ambiguity is resolved by the sending of a unique word which has a low probability of appearing in the normal bit stream. Once recognized by the receiver, it can be used to reorient the received bit stream by a simple algorithm. For example, in the 180 degree rotation case by flipping all the bits, the phase ambiguity can be resolved. This facet of phase/frequency synchronization was not implemented but could easily be employed in future versions of the design after adjusting the transmitter to transmit the unique word after every integer n data symbols. The transmission of the unique word does reduce the throughput of the system but far less than the pilot symbols used in fading channels to maintain carrier phase/frequency synchronization.

A simplified example of the operation of the carrier phase/frequency synchronization circuit for a static phase error of $\pi/8=0.393$ in a noiseless environment is depicted in Figure 20. The upper scatter plot shows the received constellation before rotation. The lower scatter plot shows the constellation after rotation by the phase/frequency synchronization circuit. The output of the phase error detector is depicted in Figure 21 and shows the critically damped second-order response of the loop filter as it forces the error to zero.

The introduction of a phase ramp error to this synchronization circuit is more complicated. If the response of the loop filter is too slow to prevent transition into another decision region, then the constellation will likely not stabilize. If the loop filter is too fast, it will be overly sensitive to noise in the received circuit. This relationship, controlled by the time-bandwidth product of the loop filter, is discussed further in Appendix A. Overall, the synchronization circuit has a narrow range of effectiveness for correcting frequency errors. It is difficult to statically display this operation as initially both the received signal constellation and rotated constellation are rotating. Subsequently, the rotated constellation returns to the same constellation pictured in the top of Figure 20.

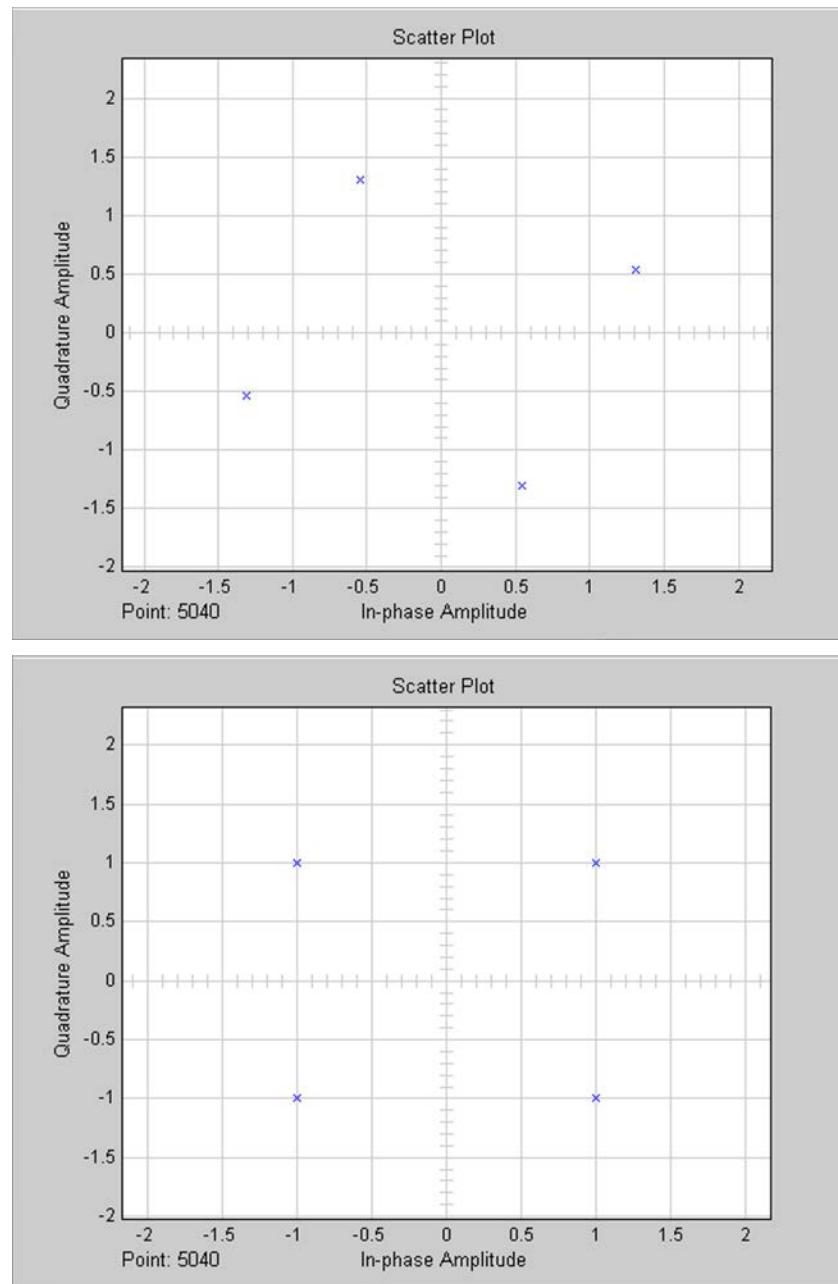


Figure 20. Received signal constellation before and after rotation by carrier phase/frequency synchronization circuit.

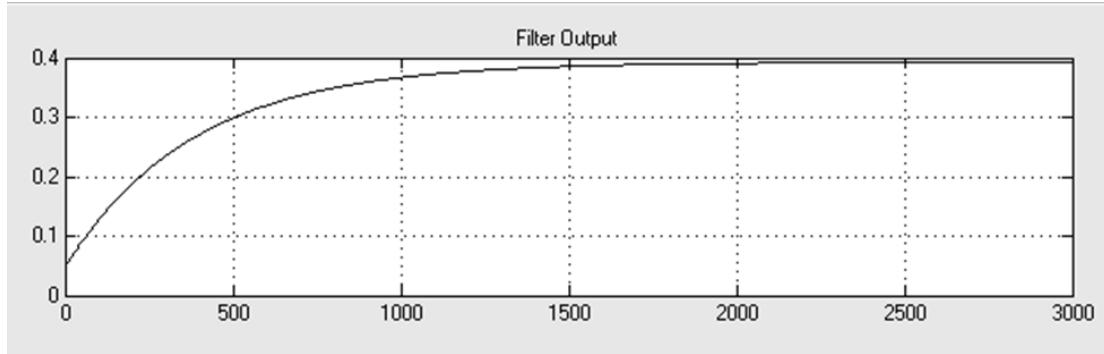


Figure 21. Output of the phase error detector.

The received constellation as shown in Figure 22 continues to rotate, giving no indication that the received signal is a QPSK signal. The input and output of the loop filter as seen in Figure 23 demonstrates that while the phase error seen in the input is driven to zero, the output of the loop filter stabilizes to the non-zero value, resulting in a rotation which matches the received signal, correcting the frequency error.

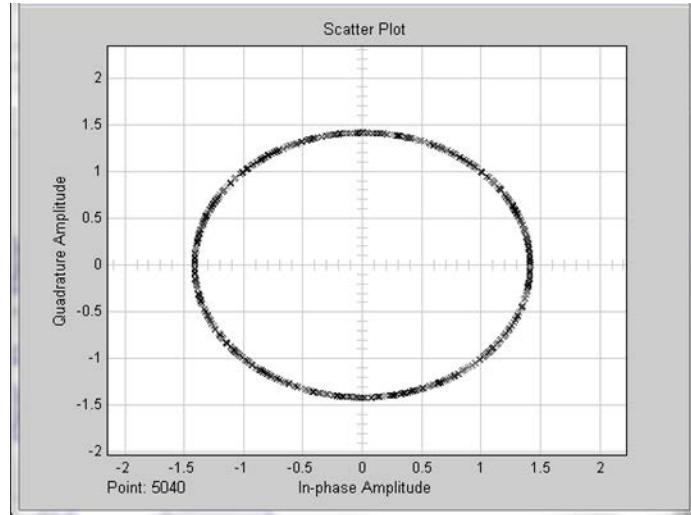


Figure 22. Received signal constellation in the case of frequency error.

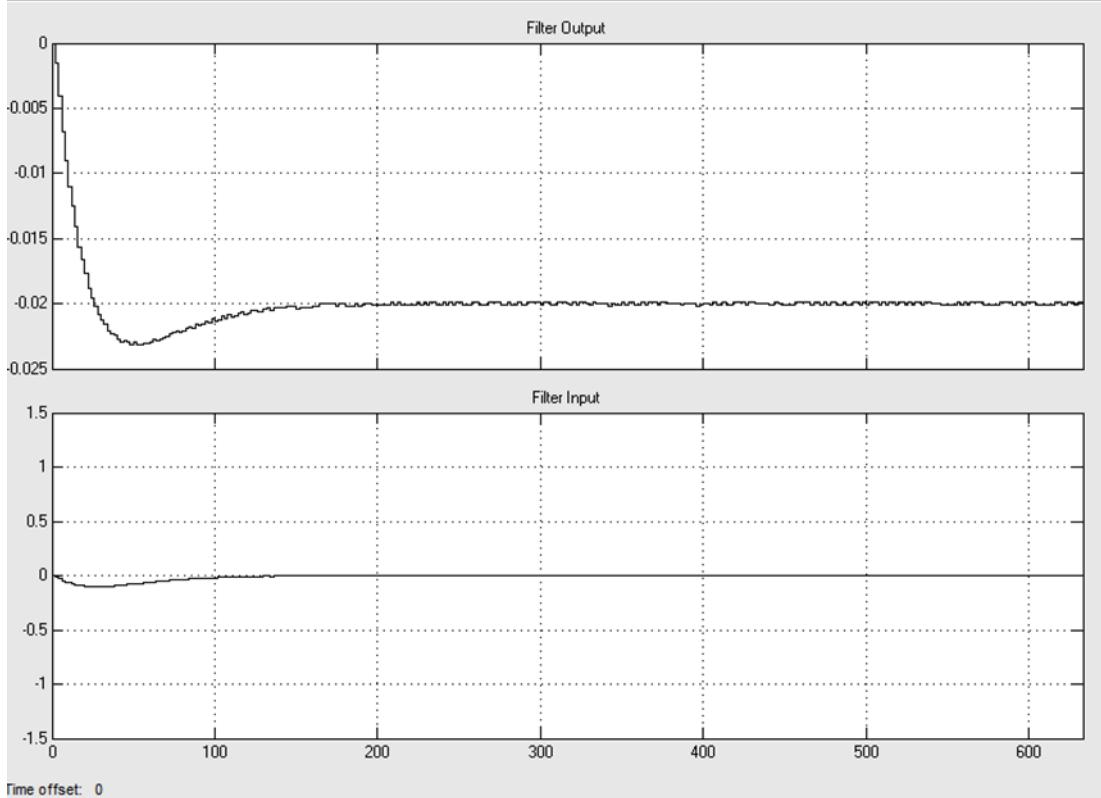


Figure 23. Output and input of loop filter in case of ramp phase error.

Some other aspects of the phase/frequency synchronization circuit impact the design. The synchronization circuit operates at a rate of one symbol per sample. The heuristic phase detector requires that the decision associated with the rotated MF outputs be matched; e.g., if there is a delay between MF output and the associated decision, the same delay must be on the heuristic phase detectors connections to the MF outputs. Fortunately, the experience gained in implementing the phase/frequency synchronization circuit was useful in the implementation of the timing synchronization circuit.

E. QPSK SYMBOL TIMING SYNCHRONIZATION CIRCUIT

The impact of symbol timing error on the amplitude of the decision statistic presented to the threshold detector was discussed in Chapter II. The purpose of the symbol timing synchronization circuit is to use the received signal to estimate the phase and frequency of the clock used in the transmitter. The purpose of synchronizing these clocks in the transmitter and the receiver is to ensure that the MF output is sampled at the

ideal time, which minimizes the impact of noise on the decision statistic [18]. Additionally, when Nyquist pulses are used to mitigate inter-symbol interference (ISI) the ideal sampling time is also the instant where there is theoretically no ISI. For example, in Figure 24 the scatter plot shows the output of the MF for a squared-root raised cosine pulse, with a roll-off of 50%, sampled at the ideal time, in a receiver on a noiseless channel. In contrast, in Figure 25 the scatter plot shows the same output sampled at the inopportune time resulting in a significant spreading of the constellation points as a result of ISI.

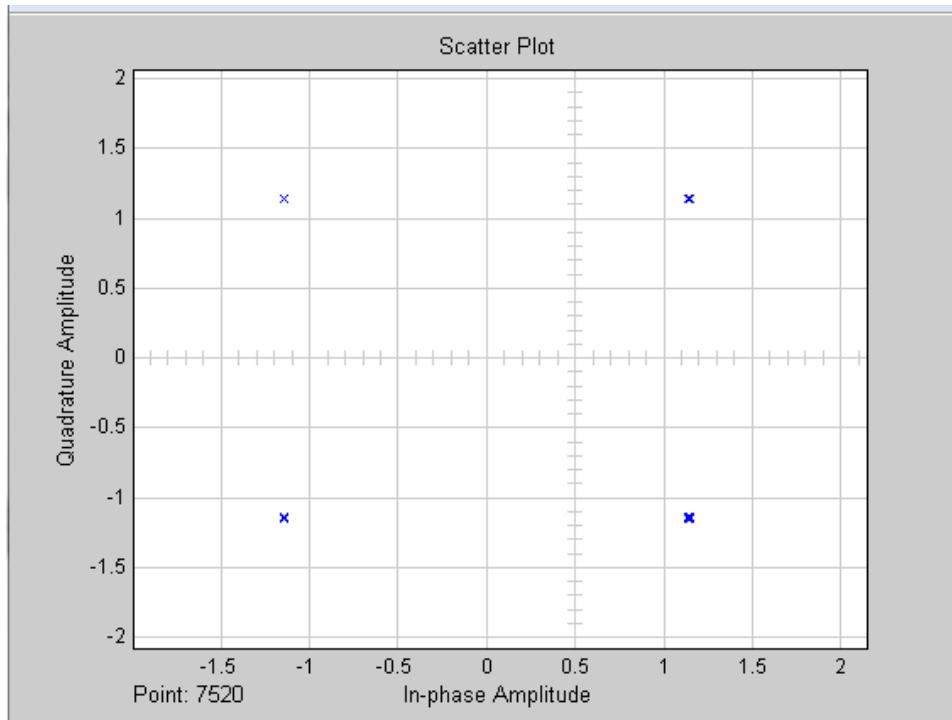


Figure 24. Constellation from sampling MF outputs with ideal timing.

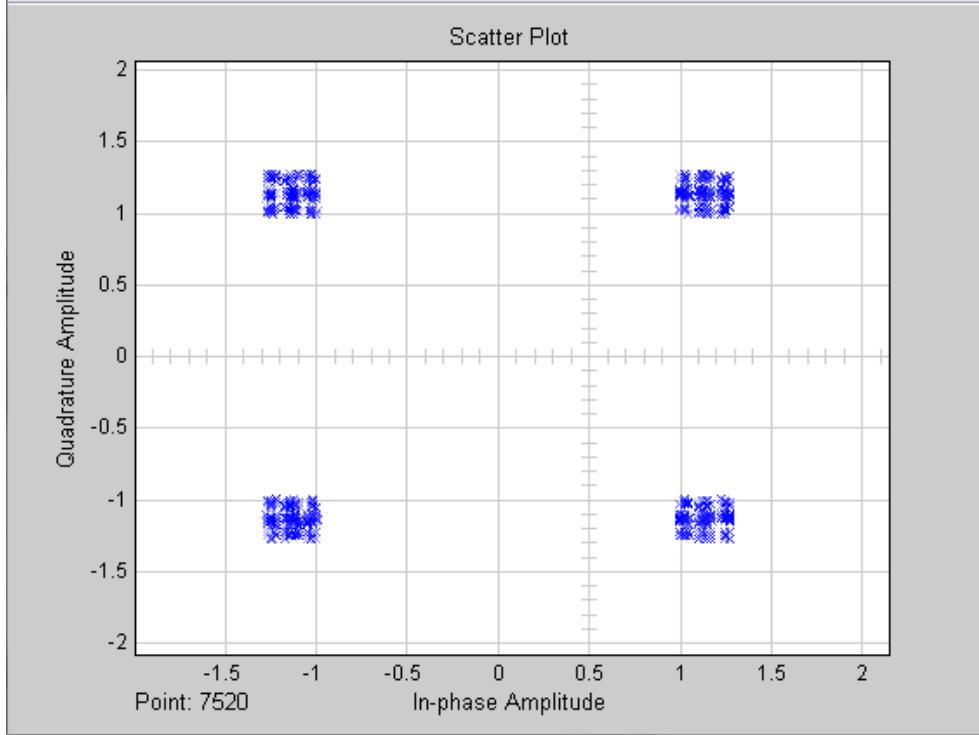


Figure 25. Constellation from sampling MF outputs with non-ideal timing.

Referring back to Figure 5, where a segment of a BPSK receiver was shown, there is a sample-and-hold element which was notionally triggered by f_{samp} . In a realistic receiver, a timing clock with frequency f_{samp} is the source of identifying when to trigger the sample-and-hold operation. This timing clock is controlled by the symbol timing PLL. The other two general elements in the symbol timing PLL are the timing error detector and the loop filter. In a discrete-time timing synchronization circuit, there are other elements based on which of several available methods are used to implement the circuit.

1. Timing Error Detector

The timing error detector (TED) measures the amount of timing error present in the outputs of the MF to generate an error signal to send to the loop filter. In general this means that the TED updates the timing error estimate once per symbol. There are many methods to estimate the timing error and, therefore, many different ways to implement a timing error detector. In one type of TED, the time derivative of the MF output is

evaluated with the understanding that at the ideal sampling time the slope should be zero. This TED is called a Maximum-Likelihood Timing Error Detector. Another type of TED uses the slope between two consecutive samples as an estimate for the slope at the sampling time. Due to the use of time differences to calculate the slope, this TED is called the Early-Late Timing Error Detector. A third type of detector uses the zero crossings that occur when adjacent symbols cause a zero crossing in the MF outputs, called transition. Due to the symmetry of the pulses used in communications, when sampling the MF output at a rate of two samples per symbol and every other symbol is a zero crossing, the middle sample is at the correct timing instant. For a Zero Crossing Timing Error Detector (ZCTED) to function, it first requires a transition in the symbols with an associated zero-crossing. No transition results in a timing error calculation of zero. The ZCTED is also a decision directed TED and is, therefore, impacted by correct symbol determination. This reliance on decisions means that the TED is sensitive to phase error in the received signal. The final type of TED being introduced is the Gardner TED (GTED) which is related to the ZCTED in the sense that it also relies on finding the zero crossings. The GTED was notably designed to operate specifically with BPSK and QPSK modulations and is not decision directed [26]. Gardner proved that this TED is “rotationally invariant,” and as a result, it allows timing synchronization to be established before carrier phase synchronization [18].

For this radio design, both the ZCTED and GTED were selected because of the ease by which they can be substituted for each other in the design implementation. Both of these TEDs are designed to operate at MF output sampling rates of two samples per symbol. The ability to use either allows side-by-side comparison of the performance of both of these TEDs. To understand the manner by which these TEDs operate requires establishing some standardized notation. The output of the timing error detector $e(k)$ is the signal that is sent to the loop filter. The values from the MF output of the in-phase channel are $x(kT_s)$, where $x(kT_s)$, $x((k-1/2)T_s)$, and $x((k-1)T_s)$ refer to the current sampled MF value and the two past values. The MF outputs closest to the ideal sampling time are $x(kT_s)$ and $x((k-1)T_s)$. The MF output closest to the zero crossing in the case of a transition is $x((k-1/2)T_s)$. The actual symbols associated with $x(kT_s)$ and $x((k-1)T_s)$ are,

respectively, termed $a(kT_s)$ and $a((k-1)T_s)$ which are unknown. Estimates of their values from the decision statistics are likewise named with $\hat{a}(kT_s)$ and $\hat{a}((k-1)T_s)$. The timing error for these MF output values is determined by the value of $x((k-1/2)T_s)$ shifted in time by the timing estimate $\hat{\tau}$, expressed as $x((k-1/2)T_s + \hat{\tau})$. Its sign is corrected depending on the direction of the transition by the symbol estimates $\hat{a}(kT_s)$ and $\hat{a}((k-1)T_s)$. The timing error estimate at a specific sample index $\hat{\tau}_e(k)$ is related to the value of the MF output at $x((k-1/2)T_s)$. The relation between these quantities and how they allow an estimate of the timing error is graphically depicted in Figure 26. In the ZCTED, the direction of the transition, whether from high to low or vice-versa is corrected based on the estimate of the two symbols. Whereas in the GTED, the difference of the value at the two samples is used as in

$$ZCTED : e(k) = x((k-1/2)T_s + \hat{\tau})[a(k-1) - a(k)], \text{ and} \quad (4-6)$$

$$GTED : e(k) = x((k-1/2)T_s + \hat{\tau})[x((k-1)T_s + \hat{\tau}) - x(kT_s + \hat{\tau})]. \quad (4-7)$$

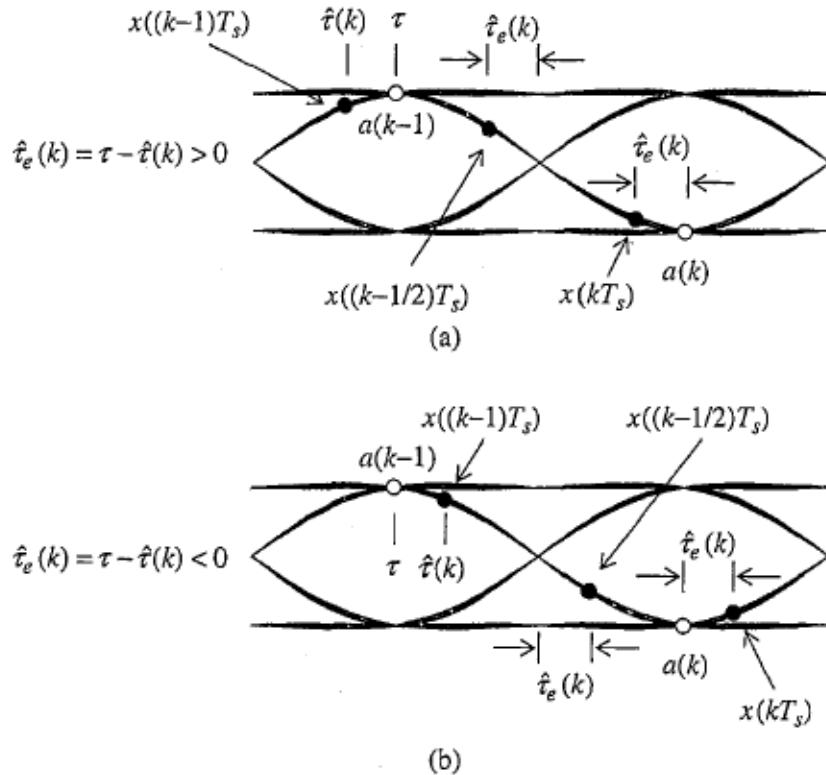


Figure 26. Examples of (a) early and (b) late timing using eye diagram. From [18].

The above equations apply to timing error detection in BPSK signals. To apply to QPSK signals, the TED equation employed is computed by summing both in-phase and quadrature-phase timing errors. There are some additional details to discuss about implementing the ZCTED or the GTED, which require understanding of two additional components, the interpolator and the interpolator control block. An explanation of these components follows a brief discussion of the loop filter.

2. Timing PLL Loop Filter

The purpose of the loop filter in this synchronization circuit is analogous to that of the loop filter in the carrier phase/synchronization circuit in that it protects the controller from the impact of errors that are the result of noise rather actual timing errors. In fact, the loop filter in this case uses the same first-order proportional plus integration transfer function. The only major difference is found in the different gains, K_p and K_o , which in the case of the timing PLL refer to the gains of the timing error detector and interpolation control circuit respectively.

3. Interpolator

The traces of the eye diagram in Figure 26 are slightly misleading in that they appear as continuous time. In a discrete-time implementation, the only values that are available are the values at the sample times. When a timing error is detected, there needs to be a means to determine the value of the output at a different sampling time. One method of accomplishing this is if the output of the timing PLL loop filter produces a control signal that modifies the clock of the analog-to-digital converter (ADC) producing the samples. This control signal adjusts the ADC timing to cause the ADC to generate samples with ideal timing. This method is similar to the carrier PLL adjusting the oscillator in the receiver. It requires crossing from discrete-time into continuous-time to implement the solution. A second method is an advanced version of connecting the sample dots called interpolation. In interpolation, the shape of the MF outputs is known in advance. When given samples of the actual MF output, the samples can be fit to the appropriate shape to allow estimation of the value at fractional intervals μ between the known sample values. An ideal interpolator has an infinite duration impulse response and

is, therefore, impractical in discrete-time. However, there are finite impulse response filters that approximate the ideal interpolation filter, which include the piecewise polynomial filters that were used [18].

The derivation of several piecewise interpolation filters exceed the scope of the documentation of this design and are well documented outside of this project. The Farrow structure for a piecewise parabolic interpolation filter was used for this design. The reader is referred to the references for more detail about these filters [18],[26]. In Figure 27, the implementation of the Farrow structure piecewise parabolic interpolator is illustrated. This interpolator operates at a sampling rate of two samples per symbol. It receives the MF output and fractional interval μ as inputs and produces the interpolated MF output value at the given fractional interval. The fractional interval value is calculated by the interpolation controller.

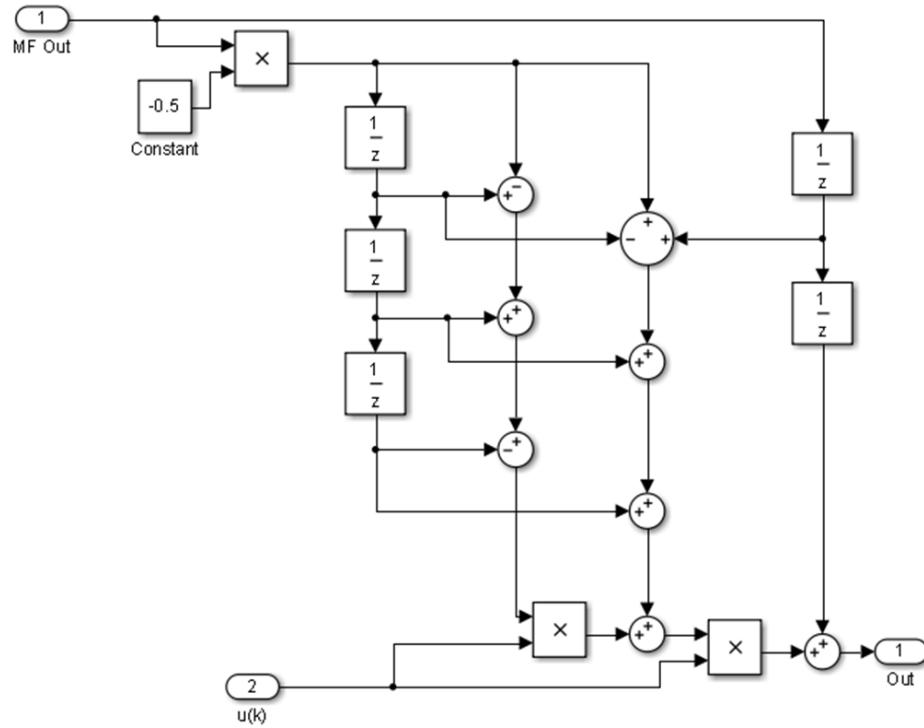


Figure 27. The implementation of a Farrow structure piecewise parabolic filter.

4. Interpolator Controller

The interpolator controller performs both the calculation of the fractional interval μ needed by the interpolator and identifies to the threshold detector which of the two samples per symbol outputs of the interpolator represent the desired time corrected decision statistic. There are two commonly used methods for interpolation control: a counter based method and a recursive based method. The counter-based method was chosen for implementation in this receiver design [18].

Understanding the operation of this circuit requires defining more nomenclature and a borrowed graphic. The counter input $W(n) = 1/N + v(n)$ where N is the number of samples per symbol and $v(n)$ is the output of the timing PLL loop filter. The next value of the counter $\eta(n+1)$ is the modulo-1 value of the current counter value $\eta(n)$ minus the value of $W(n)$, the counter input which is [18]

$$\eta(n+1) = (\eta(n) - W(n)) \bmod 1 \quad (4-8)$$

where $\bmod 1$ is defined as

$$x \bmod 1 = x - \text{floor}(x) \quad (4-9)$$

where $\text{floor}(x)$ is equal to the largest integer less than or equal to x . If the counter underflows, then index n is the basepoint index $m(k)$ which identifies the interpolator value associated with the time corrected sampling instant. The relationship between the available samples, desired interpolants, and the modulo-1 counter contents for an interpolator operating at a sampling rate of four samples per symbol is depicted in Figure 28 [18]. Depicted in Figure 29, an inset of Figure 28, is the value of $\mu(k)$ calculated directly from the counter value at the basepoint index with the following counter value as [18]

$$\mu(m(k)) = \frac{\eta(m(k))}{1 - \eta(m(k) + 1) + \eta(m(k))} = \frac{\eta(m(k))}{W(m(k))}. \quad (4-10)$$

In implementing the computation of the fractional interval, it is important to remember that Equation (4-10) is only valid at the basepoint index. Therefore, if the value is

continuously calculated, it must only be passed to the interpolator once per symbol and its value held until another valid recalculation can be performed.

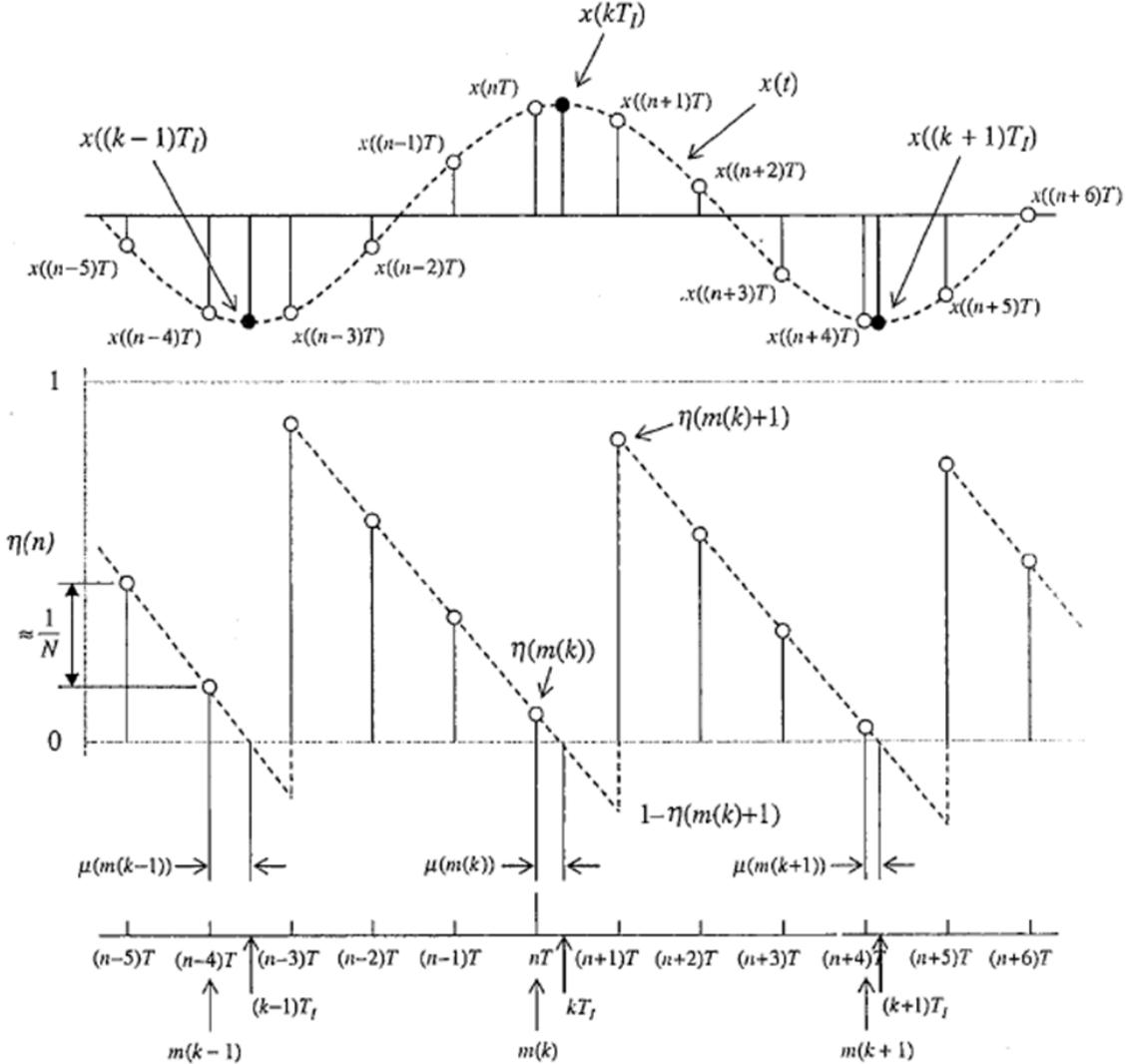


Figure 28. The relationship between the available samples, the desired interpolants, and the modulo-1 counter contents. From [18].

The implementation of a modulo-1 counter as the interpolator control is shown in Figure 30. The counter implementation follows the above description precisely. Underflow detection is accomplished by comparing the input and output of a modulo-1 operation. The division by zero protection appears again with the Simulink divide block to protect against division by zero errors. A step function is used, as with the phase error detector, to protect the calculations of fractional interval from meaningless values during

system initialization. The enabled subsystem is the mechanism by which the modulo-1 counter only updates the fractional interval value at the symbol rate as determined by the underflow strobe. The strobe, or underflow condition of the modulo-1 counter, is an output of the interpolator control which is also needed by other system elements.

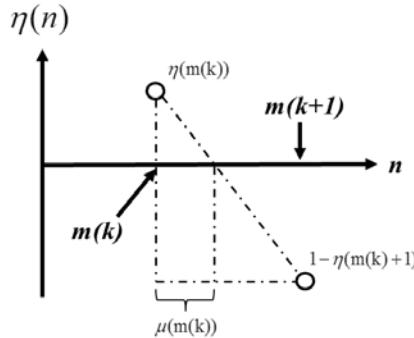


Figure 29. Graphical depiction of the similar triangles used in fractional interval calculations. After [18].

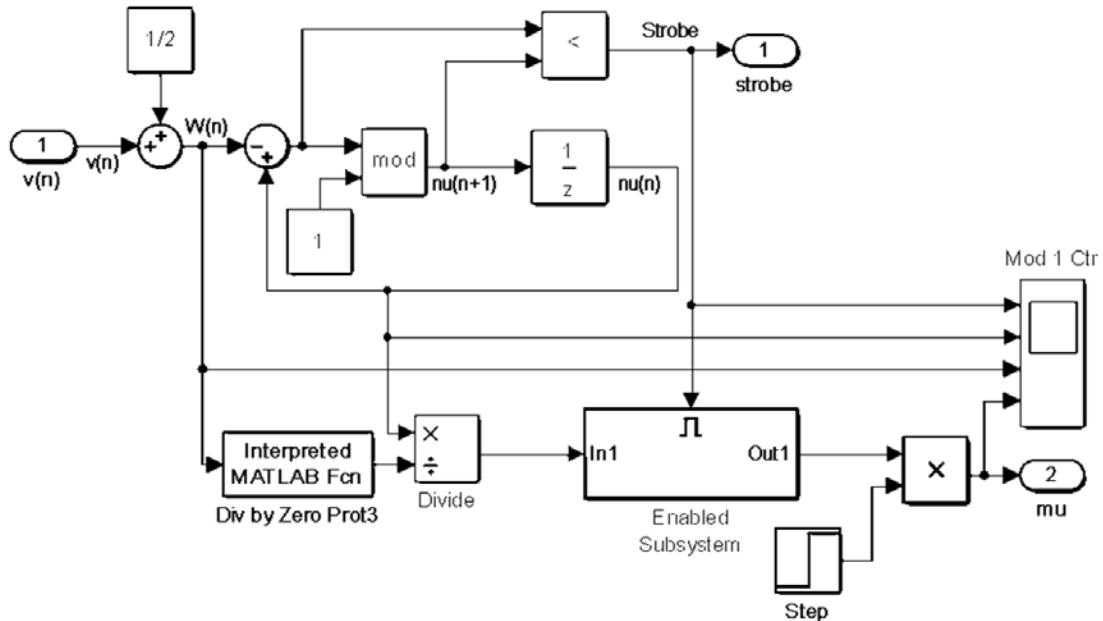


Figure 30. The implementation of an interpolator controller.

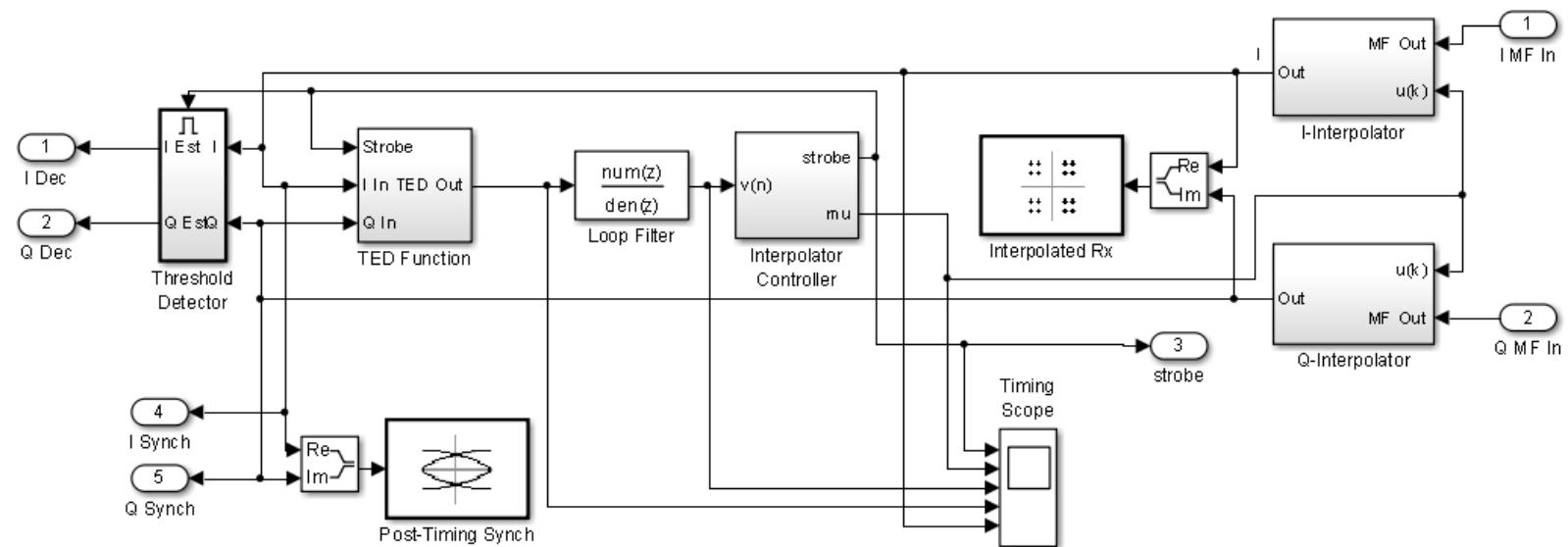


Figure 31. An illustration of the complete timing synchronization circuit.

5. Putting It Together

In Figure 31, the entire implementation of the timing synchronization circuit is depicted. The implementations of the interpolator and the interpolator controller have been described previously. It is shown in Figure 31 that the strobe from the interpolator controller is also an output of the timing synchronization circuit. Recall that the phase error detector in the carrier phase/frequency synchronization circuit operates at a sampling rate of one sample per symbol. When the interpolator is added to the system, the output of the MF is at a rate of two samples per symbol. In order to reduce the sampling rate and identify which of the two interpolator outputs represents the decision statistic, the phase detector uses the strobe to calculate the phase error when the strobe is high and to hold its value when the strobe value is low. The strobe also has internal connections to the threshold detector and the timing error detector. The connection to the threshold detector enables and holds decisions at the correct rate of one decision per symbol and correctly identifies which interpolator outputs represents the decision statistic. The threshold detector is identical to the previous threshold detector with the exception of being enabled by the strobe signal. The strobe connection to the timing error detector serves the same function of identifying the correct sample indices at which to update the timing error estimate. However, there is a great deal of subtlety that goes into the implementation of the timing error detector.

6. The Timing Error Input Buffer

The implementation of the timing error detector remains one of the most complicated aspects of this radio design. The calculation of the timing error as described previously is relatively simple. There are two issues that arise and both result from consecutive strobe signals being either low or high. The two cases that can cause consecutive strobe signal to be equal are:

- Case 1: The error in the timing between the symbol clock in the transmitter and receiver is not a step error, but instead a ramp error resulting from frequency mismatches in the symbol timing clocks.
- Case 2: The timing error estimate is at zero or unit value and noise in the circuit, either AWGN in received signal, or even quantization noise in noiseless environment causes the estimate to go negative or above unity.

In both cases, there is good reason for a consecutive high or low strobe signal to ensure that the timing synchronization circuit can track the transmitter's timing clock. In the case of consecutive high strobes, there is an interpolant needed by the timing error detector which is never produced. In the case of consecutive low pulses, an unneeded interpolant is produced [18]. To enable the TED to deal with these issues, a TED input buffer updated based on the current and past strobe values is needed. It maintains registers for the past two interpolator values, $x((k-1/2)T_s + \hat{\tau})$ and $x((k-1)T_s + \hat{\tau})$, which are needed for calculating the timing error.

The timing error detectors input buffer has to deal with four cases related to the present and past strobe values:

- Present high strobe preceded by a low strobe,
- Present low strobe preceded by a high strobe,
- Present high strobe preceded by a high strobe, and
- Present low strobe preceded by a low strobe.

In the first two cases, the TED input buffer functions as a serial shift register by 1) shifting the value of $x((k-1)T_s + \hat{\tau})$ out of the register and replacing it with the past value of $x((k-1/2)T_s + \hat{\tau})$ and 2) shifting the current interpolator value into the register as $x((k-1/2)T_s + \hat{\tau})$. The only difference between the first two cases is that in the first case the value of the timing error is calculated. In the second case, it is not calculated but rather is set to zero. In the last two cases, only the registers are adjusted and the timing error is set to zero in both scenarios. If the TED input buffer receives consecutive high strobes, no interpolant with a zero value was produced. In this case, the $x((k-1)T_s + \hat{\tau})$ register is loaded with a zero, and the $x((k-1/2)T_s + \hat{\tau})$ register is loaded with the current interpolator output value. When the TED input buffer receives consecutive low strobes, it is because an additional unneeded interpolant was produced. In this case, both registers are held unchanged and the current interpolator value is discarded. [18]

The TED input buffer described above requires the implementation of a finite state machine to deal with each of the above cases. The TED updates can be slightly above or below once per symbol. Thus, it is difficult to implement this function in the Simulink

environment. In order to successfully implement this function, a Simulink S-function was used. The complete S function code is included in Appendix B. To use this function in Simulink, the three required inputs (the strobe value, the in-phase and quadrature interpolator values) must be multiplexed into a single signal and the strobe signal converted from a Boolean value to a double-precision number. The overall implementation of the TED is depicted in Figure 32.

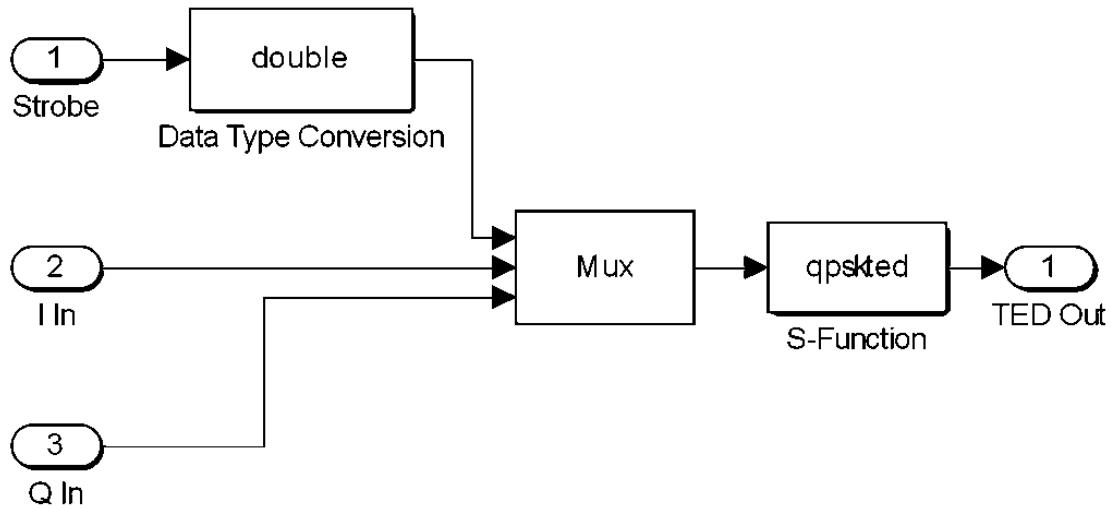


Figure 32. An illustration of the final implementation of the QPSK timing error detector.

After the completion of the timing synchronization circuit, depicted in Figure 31, the phase error detector was moved into the location of the threshold detector. This design decision simplified synchronizing the phase error detectors inputs as the interpolated MF outputs and the associated decision are both present and occur without delay in corresponding values. The modified threshold detector/phase-error detector is depicted in Figure 33.

Another challenging issue with the timing synchronization circuit is that the decisions made by the threshold detector do not occur at a set rate. When there is a symbol timing clock frequency offset between the transmitter and the receiver, there are be occasions when the threshold detector either produces consecutive decisions or when the period between two consecutive decisions is 1.5 symbol periods rather than the

standard one symbol period. These phenomena allow the receiver to match the transmitter's symbol timing clock frequency without adjusting the sampling rate of the receiver. Unfortunately, Simulink does not have any basic blocks that allow the transfer of signals to the workspace with variable sample rates or by application of a trigger. The solution was to output both the in-phase and quadrature decisions to the workspace at twice the symbol rate, along with the strobe signal. This solution allows a MATLAB script to sort through the decisions and to discard decisions without an associated timing strobe. The remaining decisions constitute the received signal. The completed receiver with the above modifications is depicted in Figure 34.

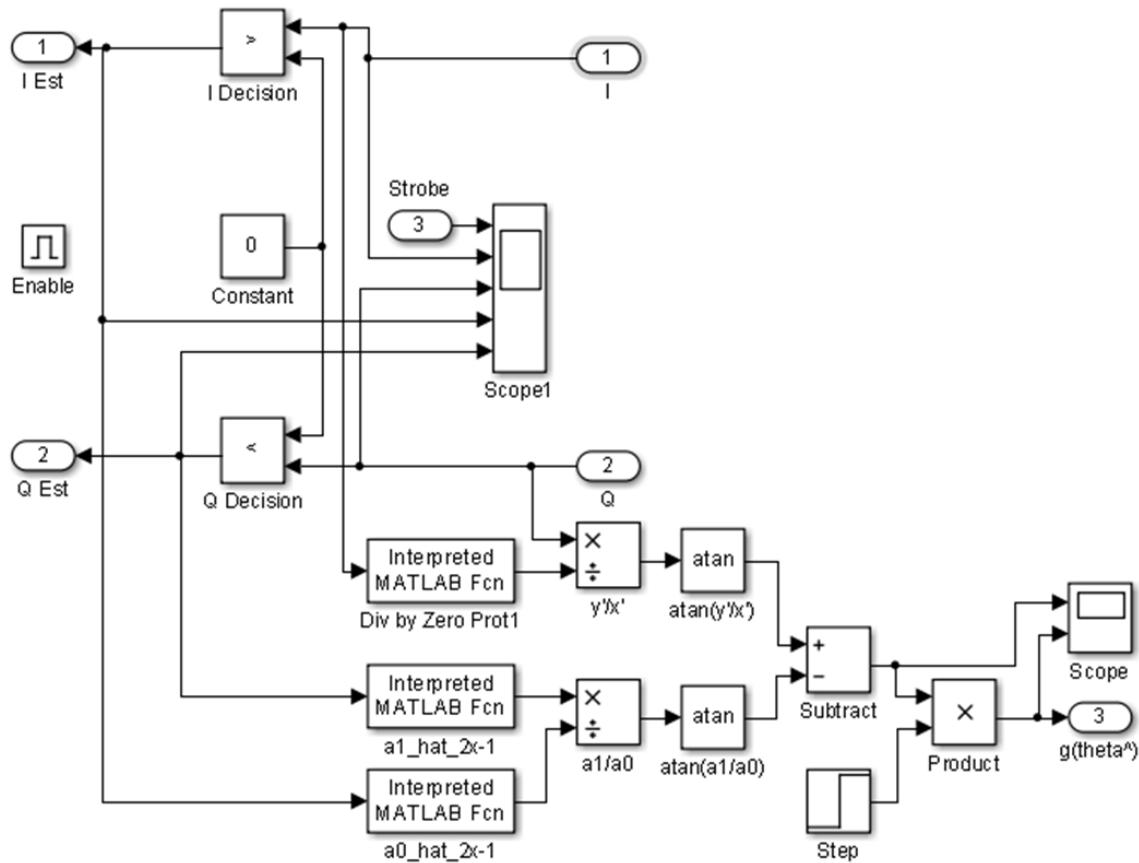


Figure 33. Modification to the threshold detector including the phase-error detector.

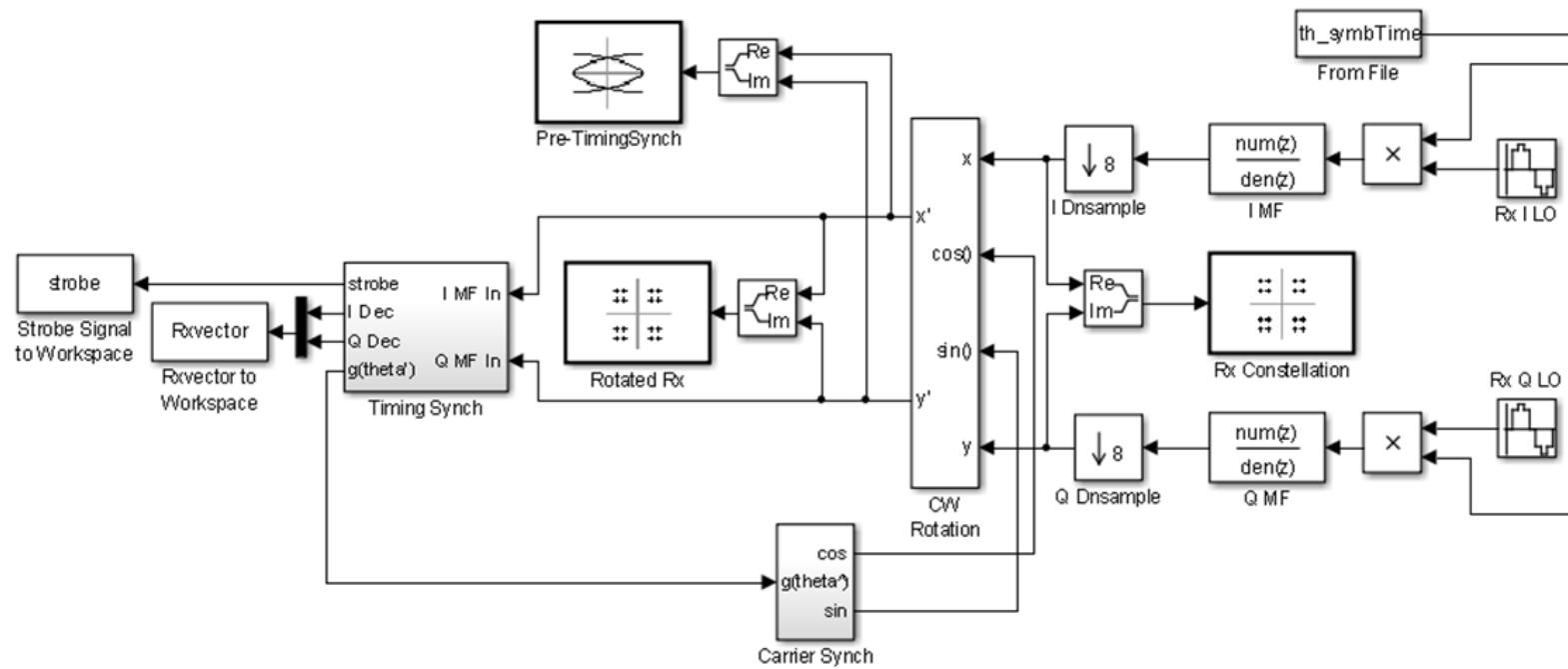


Figure 34. The complete receiver design.

To test the timing error detector, a unit delay was introduced to the impulse train going to the transmitter's pulse shaping filter. This unit delay simulates a step error to the timing synchronization circuit. The result, as depicted in Figure 35, was another second order response similar to the response that occurred at system initialization. Of note in the illustration is that the strobe signal is depicted at a scale that prevents visualization of its transitions. To simulate a ramp error, the symbol rate of the transmitter was adjusted to a rate of 0.50005 symbols per second, 0.01% more than the nominal rate of 0.500 symbols per second. The output of the interpolator controller shown in Figure 36 shows the incremental adjustments of the symbol timing synchronization circuit that eventually resulted in the fractional interval exceeding one and wrapping back to zero. When the fractional interval exceeds one, it results in a consecutive low strobe value and signifies that the decision has been postponed by half a symbol period to correct for the timing mismatch between the transmitter and receiver, depicted in Figure 37.

With the timing synchronization circuit complete, the initial design was complete and the circuit was prepared for performance testing. Before testing, there was a small change that was implemented during the design of the symbol timing circuit that requires some discussion.

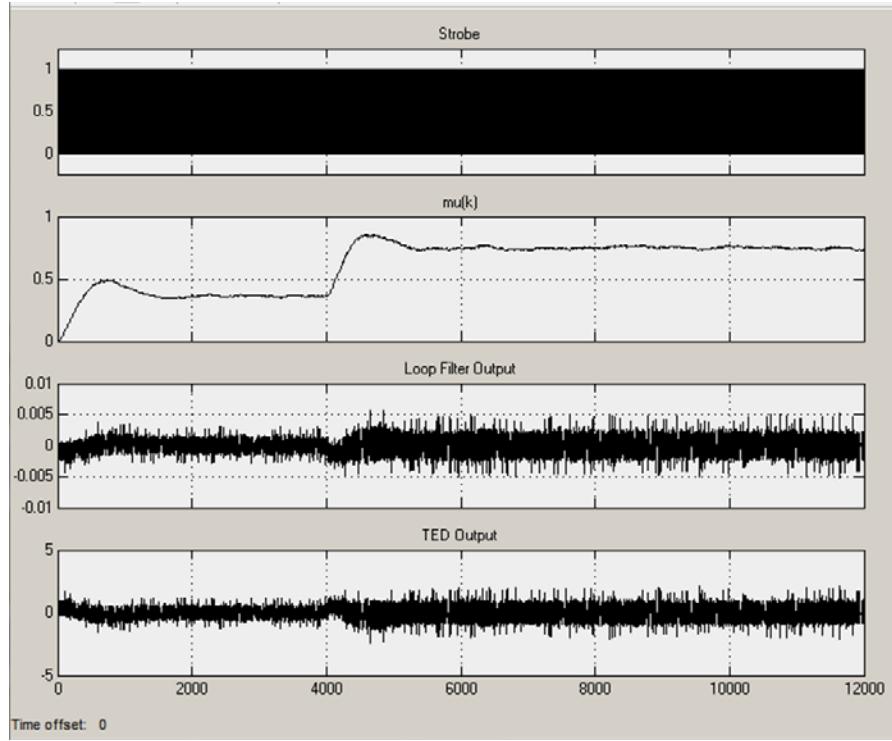


Figure 35. The output of the timing synchronization circuit components for a step error at sample index $n=4000$.

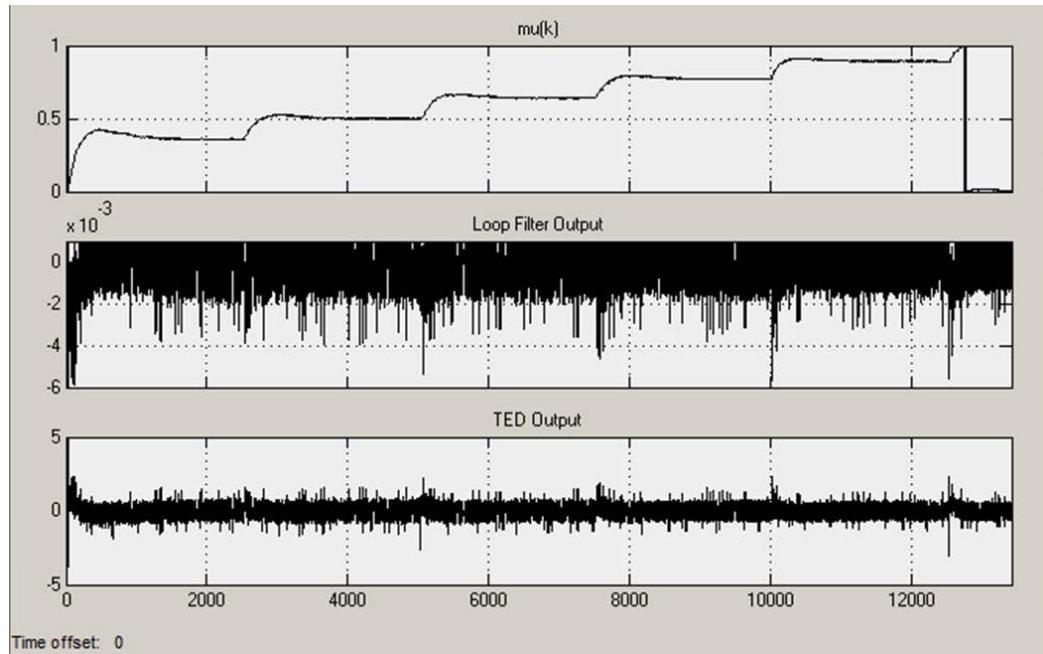


Figure 36. The response of the timing synchronization circuit to a symbol timing frequency mismatch between the transmitter and receiver.

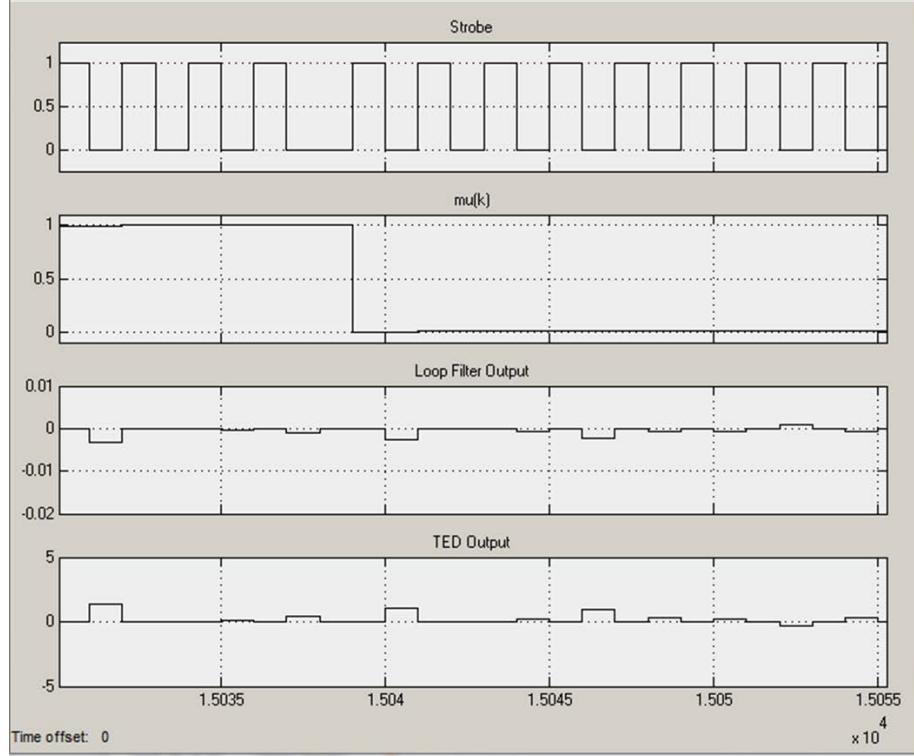


Figure 37. Depiction of the timing synchronization circuit delaying a decision in order to match a transmitter symbol clock with a frequency offset.

F. PULSE SHAPING FILTERS

For most of the design work, rectangular pulse shaping was employed because the output of the match filter for rectangular pulse shaping is an easily visualized triangular function. Unfortunately, the rectangular pulse is spectrally inefficient, as its Fourier transform is a sinc function. This is never a popular choice for use in practical satellite communication systems to limit interference with adjacent signals on the satellite transponder. In addition to being bandlimited, another attractive feature for a pulse shape is that the pulse shape prevents ISI. A popular pulse with no ISI, i.e., a Nyquist Pulse, is the raised-cosine pulse shown in Figure 38. The raised-cosine is a popular pulse shape as it is spectrally efficient. The zeros in the time domain function occur at the sampling time of adjacent signals, which results in no ISI, as depicted in Figure 39 [20]. Since the raised cosine pulse is strictly bandlimited, theoretically, it requires infinite time support. When it comes to the decision statistic, the pulse shape seen by the threshold detector is the result of the impulses in the transmitter being filtered by the pulse shaping filter in the

transmitter, the channel itself, and the pulse shaping filter in the receiver. The final pulse, which is the multiplication of these transfer functions in the frequency domain (assuming an ideal channel with $H(f)=1$), is a Nyquist pulse. Therefore, the pulse-shaping filter that should be employed in the transmitter and MF employed in the receiver should both have impulse responses equal to the squared-root raised cosine pulse (SRRC) [20]. The SRRC is defined in the frequency and time domains as [18]

$$P(f) = \begin{cases} \sqrt{T_s} & 0 \leq |f| \leq \frac{1-\beta}{2T_s} \\ \sqrt{T_s} \cos\left(\frac{\pi|f|T_s}{2\beta} - \frac{\pi(1-\beta)}{4\beta}\right) & \frac{1-\beta}{2T_s} \leq |f| \leq \frac{1+\beta}{2T_s}, \text{ and} \\ 0 & |f| > \frac{1+\beta}{2T_s} \end{cases} \quad (4-11)$$

$$p(t) = \frac{1}{\sqrt{T_s}} \frac{\sin\left(\pi(1-\beta)\frac{t}{T_s}\right) + \frac{4\beta t}{T_s} \cos\left(\pi(1+\beta)\frac{t}{T_s}\right)}{\pi t \left[1 - \left(\frac{4\beta t}{T_s}\right)^2\right]}, \quad (4-12)$$

where T_s is the symbol period and β is the roll off factor, which is between zero and one. This continuous time pulse can be transformed into a discrete-time pulse using the impulse invariance technique (sampling and scaling continuous time filter impulse response to form discrete time filter impulse response) if the sample rate is greater than twice the highest frequency, which from (4-11) is $(1+\beta)/T_s$. If the sample rate $1/T_s$ is defined as N times the symbol rate, as in $T_s/T = N$, then a discrete time version of (4-12) results from substituting $t=nT$ and scaling the pulse amplitude by \sqrt{T} as [18]

$$p(nT) = \frac{1}{\sqrt{N}} \frac{\sin\left(\pi(1-\beta)\frac{n}{N}\right) + \frac{4\beta n}{N} \cos\left(\pi(1+\beta)\frac{n}{N}\right)}{\pi n \left[1 - \left(\frac{4\beta n}{N}\right)^2\right]}. \quad (4-13)$$

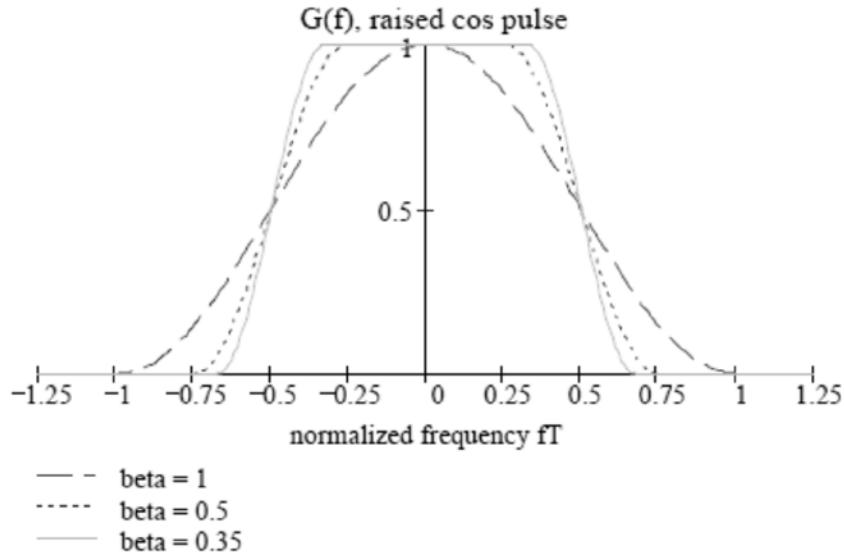


Figure 38. Illustration of the frequency spectrum of a raised-cosine pulse. From [27].

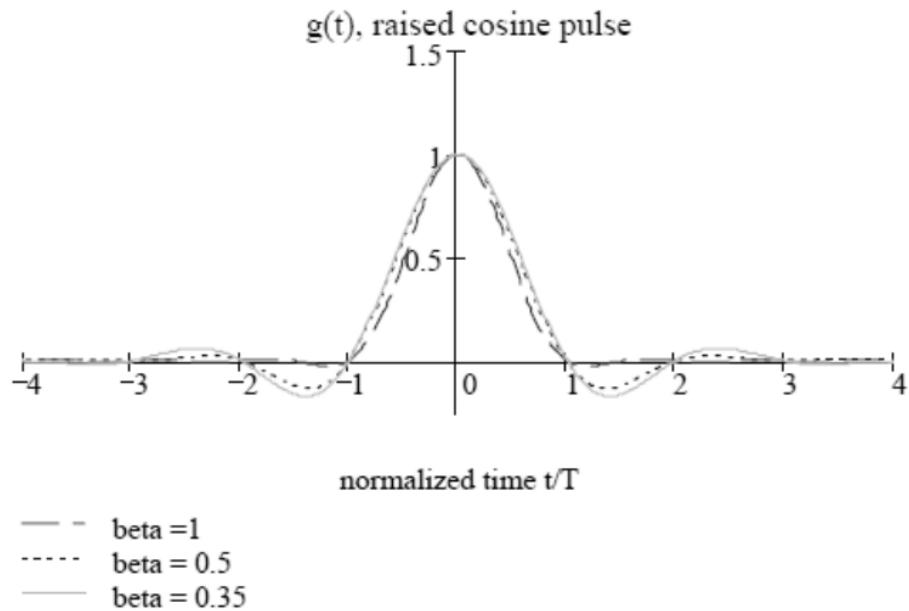


Figure 39. A graph of the time-domain raised-cosine pulse. From [27].

Before implementing the above pulse shaping into the design, it is important to highlight that in pulse shaping with the SRRC pulse shape that adjacent symbols must overlap. In fact, the time pulse has to be windowed to enjoy finite time support. As a result, the more adjacent symbols that overlap the larger the window. The larger the

window, the greater the time support required and the greater the time support the smaller the bandwidth of final symbol. Since the pulse now only approximately satisfies the Nyquist criteria, there is a finite amount of ISI present at the sampling time. It has been shown that the amount of ISI also decreases with increased window sizes and overlapping, such that with a pulse overlapping with the six previous and the six following pulses, the ISI at the sampling time peaks at 0.27% [18].

The implementation of pulse shaping occurred in the associated MATLAB script which parameterized the simulation blocks. This implementation allowed changing between rectangular and SRRC shaping to be a matter of commenting and uncommenting adjacent blocks of code. Also, by coding the implementation of the SRRC pulse shaping, some parameters can easily be changed, e.g., the length of the windowing for the SRRC pulse shape.

The designed radio is a functional, realistic QPSK receiver model with optional rectangular or SRRC pulse shaping and both carrier and timing synchronization circuits. Performance testing of this model and comparisons against the performance of the optimum QPSK receiver are discussed in the next chapter.

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V. SINGLE RECEIVER PERFORMANCE

A. PERFORMANCE WITH SINGLE SIGNAL IN AWGN

To test the design, it is important to clarify the parameters for the transmitter and receiver during each test as well as what assumptions were made during the testing. Several common assumptions are made throughout all of the performance tests. The first assumption is that the BER calculations discount errors that occur during the initialization of the receiver. This assumption is reasonable. Even in burst transmissions, such as time division multiplexing, the receiver is provided the opportunity to gain coherency with a combination of a training sequence and unique words [19]. This leads to the second assumption. The communication protocol employs a method to initially resolve the issue of phase ambiguity, perhaps with the unique words described earlier [18]. Any phase ambiguity which arises after initialization is discussed further if it occurs.

Before the first tests, we should note that the BER of a coherent QPSK signal is described by Equation (2-15), is graphically depicted alone in Figure 40, and appears in future BER plots as a reference. For the first performance test, the receiver has no carrier frequency or phase offsets and no timing frequency offset. Timing phase is offset only at initialization with no additional error introduced. A transmission is produced by the transmitter of sufficient length to result in a sufficient number of errors by which to generate reasonable confidence in the receiver's performance. For example, in the first trial the E_b/N_o was set to 1 dB, and the transmitter generated a transmission of 2000 random symbols. The receiver was then run, and the output was compared to the original transmission to calculate a BER. In order to ensure that the result is reasonable, the number of errors seen is displayed in Figure 41 along with a binomial probability density function of the theoretical BER. The results of 12 simulations at various values of received signal E_b/N_o is shown in Table 1. The number of symbols for each simulation is included to allow calculation of the significance of each result. In Figure 42, the results are plotted with the optimum coherent demodulator. The end result is that the designed receiver performed essentially at optimum levels when taking into account the statistical significance of the results.

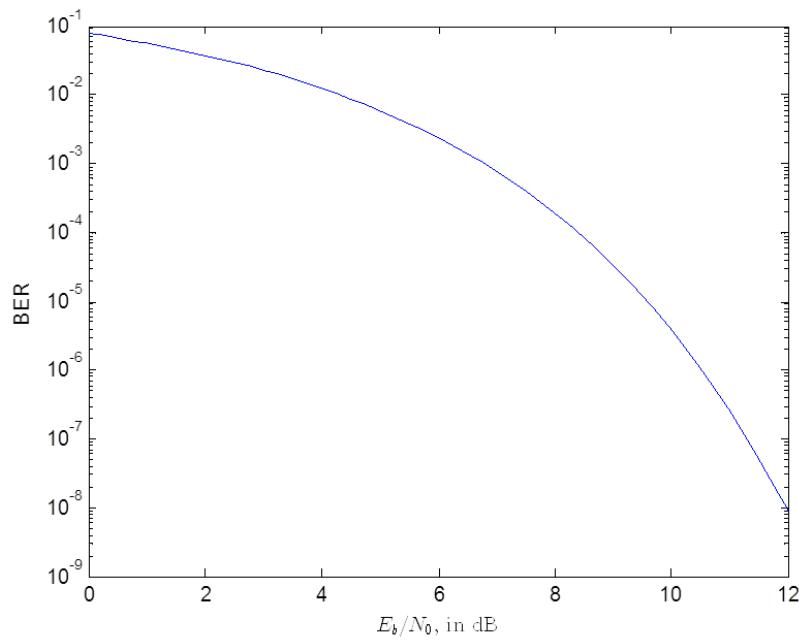


Figure 40. The BER of coherent QPSK from Equation (2-15).

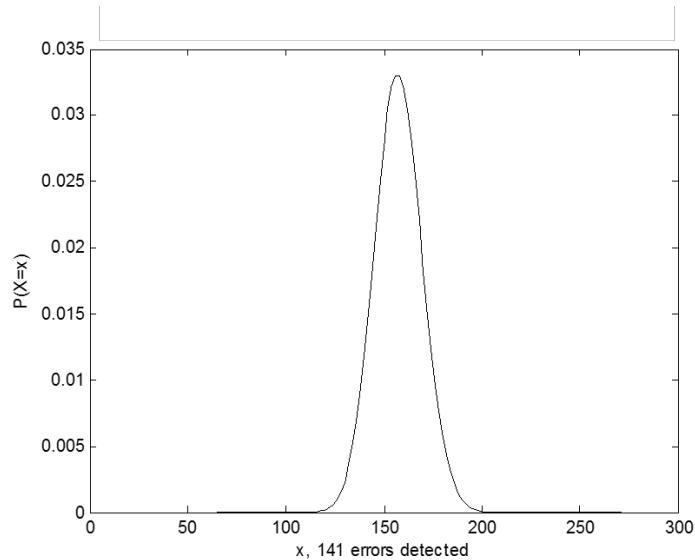


Figure 41. The feedback provided by BER checking script to ensure the confidence level of the results.

Table 1. Discrete-time receiver BER performance for various received E_b/N_o values.

E_b/N_o (dB)	Number of Bits	Number of Errors	BER
1	2973	181	6.09E-02
2	5973	242	4.05E-02
2.5	8973	282	3.14E-02
3	8973	231	2.57E-02
3.5	8973	170	1.89E-02
4	19973	289	1.45E-02
5	24973	181	7.25E-03
6	39973	92	2.30E-03
7	79973	75	9.38E-04
8	159973	38	2.38E-04
9	499973	17	3.40E-05
10	1999948	10	5.00E-06

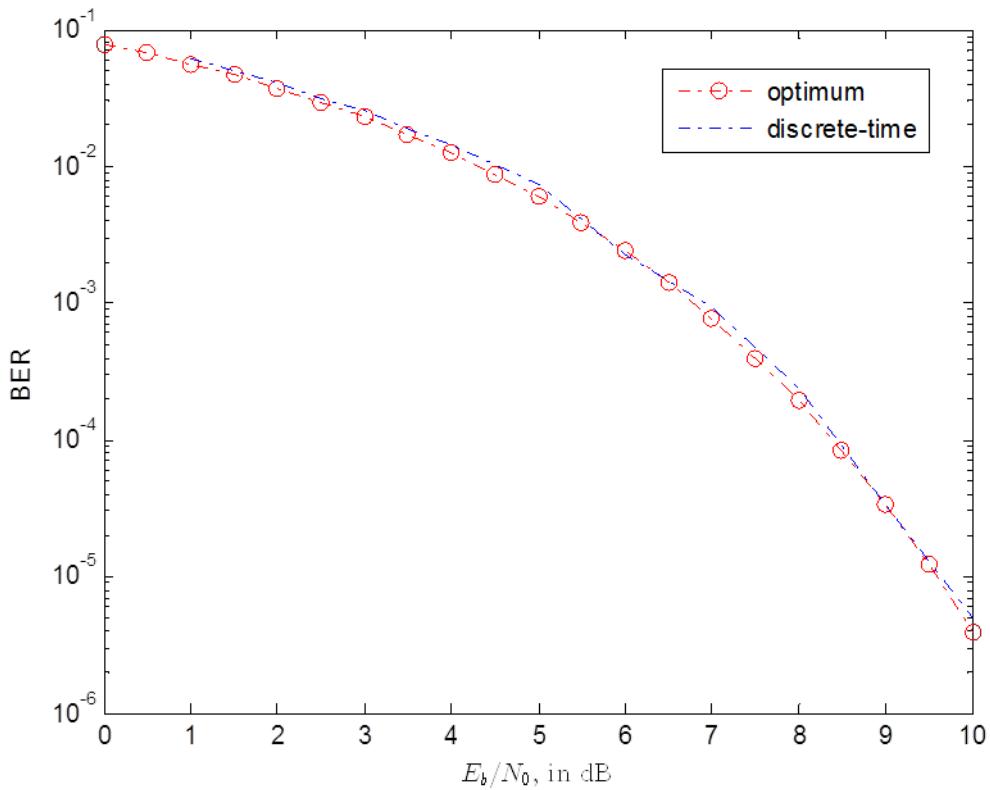


Figure 42. Plot of discrete-time receiver BER performance versus optimum detector.

For the next performance test, more realistic values were used for the receiver's parameters to better simulate real world performance. The timing clock and carrier frequencies between the transmitter and receiver were offset. Technical specifications of the Comtech DMD2050E Universal Satellite Modem, a commercial off-the-shelf satellite modem, list the precision of the data clock as 0.05 parts per million of stability [28]. This is three orders of magnitude more precise than the ramp error initially used in testing the timing synchronization circuit in the previous chapter. For the worst case scenario, the next tests increase this error twentyfold to one part per million of stability. This frequency offset was applied to both the timing clocks and the oscillators. Additionally, an initial phase error of $\pi/8$ at the receiver was assumed. More phase error was not introduced to avoid locking in at another phase due to the 90, 180, and 270 degree ambiguity discussed when designing the phase error detector. Testing focused on a more realistic E_b/N_o value range between two and eight dB. The results of this testing, which is also graphically depicted with the performance curve of the optimum detector in Figure 43, is contained in Table 2. Even when using real-world performance parameters such as clock error, the receiver performs at near optimum levels.

Table 2. Realistic receiver BER performance for various received E_b/N_o values.

E_b/N_o (dB)	Number of Bits	Number of Errors	BER
2	8973	373	4.16E-02
2.5	8973	300	3.34E-02
3	8973	239	2.66E-02
3.5	8973	152	1.69E-02
4	19973	269	1.35E-02
5	24973	157	6.29E-03
6	39973	116	2.90E-03
7	249973	212	8.48E-04
8	249973	61	2.44E-04

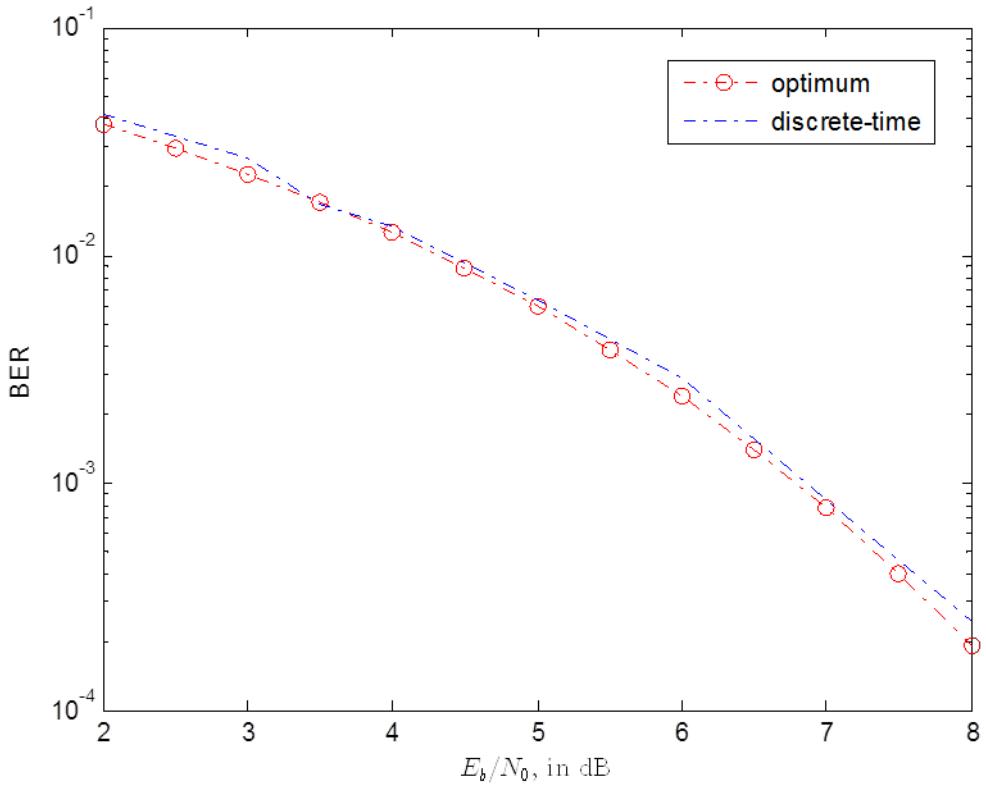


Figure 43. Plot of realistic receiver BER performance versus optimum detector.

B. PERFORMANCE OF HIGH POWER SIGNAL DEMODULATION WITH CO-CHANNEL INTERFERENCE IN AWGN

Testing the receiver's performance in the demodulation of a high power signal where an interfering co-channel low power signal is present demonstrates the potential utility of the design for further research. The E_b/N_o of the HP signal is set at 10 dB, and subsequently, the noiseless LP signal is attenuated to the desired level and added to the HP and noise signal. The reconfiguration of the transmitter to perform this function is shown in Figure 44. With the E_b/N_o of the HP signal held constant at 10 dB, the attenuation of the low power signal was adjusted incrementally from 10 dB to 0 dB. At each increment, the BER performance of the receiver in demodulating the HP signal was recorded. The results of this test are listed in Table 3 and graphically depicted along with the theoretical curve in Figure 45. The curve results from a common approximation used

in calculating the impact of co-channel interference, which treats the interfering signal as another form of AWGN which adds to the AWGN due to thermal noise. In this approximation, the resulting BER is described by

$$BER = Q\left(\sqrt{\frac{2}{\frac{N_o}{E_b} + \frac{I}{C}}}\right), \quad (5-1)$$

where the interference-to-carrier ratio I/C is added to the denominator in Equation (2-15) [29]. Since the HP signal's E_b/N_o is held at 10 dB and the interfering signal is at unit power, Equation (5-1) reduces to

$$BER = Q\left(\sqrt{\frac{2}{0.1 + \frac{I}{C}}}\right). \quad (5-2)$$

This approximation is also depicted in Figure 45 along with the results of the simulation.

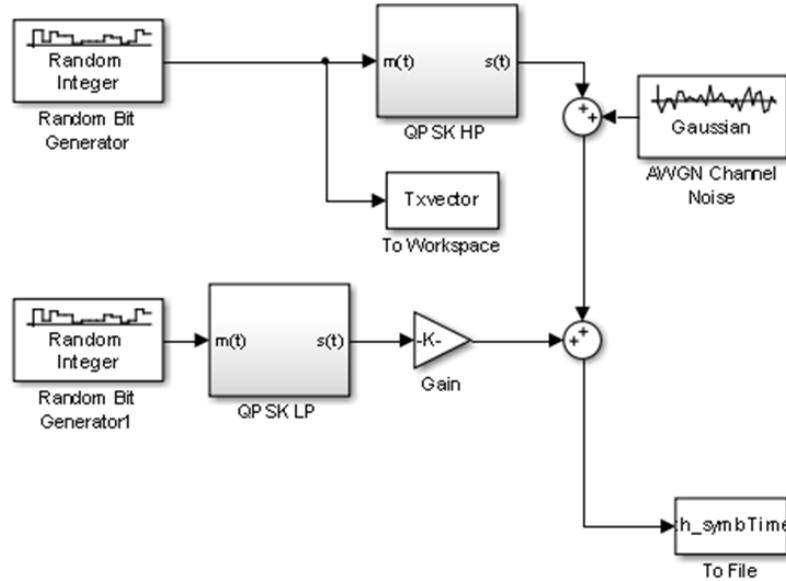


Figure 44. Reconfiguration of QPSK transmitter to generate combined HP and LP signal.

Table 3. HP Signal BER in presence of co-channel interference from LP signal.

LP/HP (dB)	Number of Bits	Number of Errors	BER
-10	1249972	18	1.44E-05
-9	999973	23	2.30E-05
-8	999973	59	5.90E-05
-7	999973	161	1.61E-04
-6	499973	218	4.36E-04
-5	249973	388	1.55E-03
-4	99973	516	5.16E-03
-3.5	49973	550	1.10E-02
-3	49973	1454	2.91E-02
-2.5	9973	2997	3.01E-01
-2	9973	2216	2.22E-01
-1.5	9973	2763	2.77E-01
-1	9973	2677	2.68E-01
0	9973	2868	2.88E-01

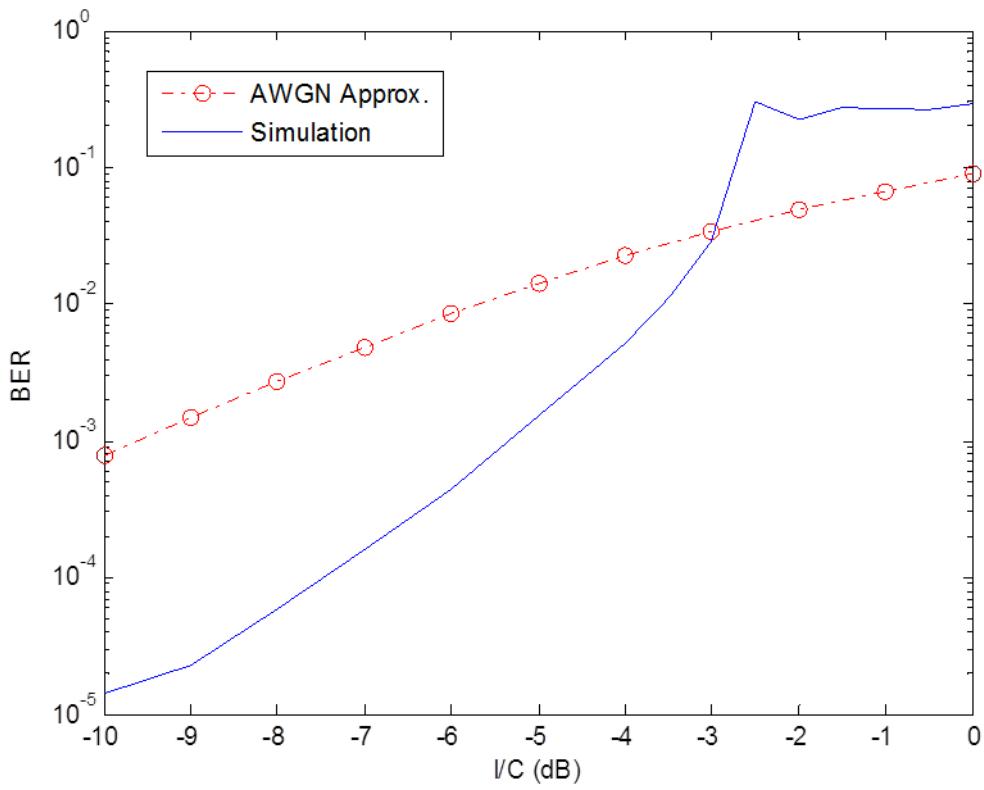


Figure 45. BER of HP signal demodulation in presence of co-channel LP interference.

Cursory examination of Figure 45 shows that the Gaussian approximation of Equation (5-2) forms an upper bound on the BER performance as seen in the simulation for I/C levels less than 0.5. An anomaly in the BER occurs at an I/C level of 0.5 where the simulated BER exceeds that of the approximation. By repeating the simulation for a lower I/C value of negative four dB and comparing it to the simulation of the I/C value of 0.5 we can observe what is happening. As depicted in Figure 46, at the I/C value of 0.5, the constellation points of the LP signal have enough energy to intrude into the adjacent HP signal decision regions, while at lower I/C levels they largely do not. It is reasoned that the sharp departure from the AWGN model that occurs is related to differences in phase between a co-channel interference signal and AWGN. In AWGN the phase of the noise is uniformly random. In the co-channel interference signal the phase is concentrated near the constellation points of the LP signal. Watching the received constellation diagram also reveals that at the I/C value of 0.5, the output constellation clearly loses carrier phase lock and occasionally rotates and locks in on an ambiguous phase. It is reasonable to assume that at an I/C level of 0.5 that the LP signal has entered a range where it very effectively jams the HP signal.

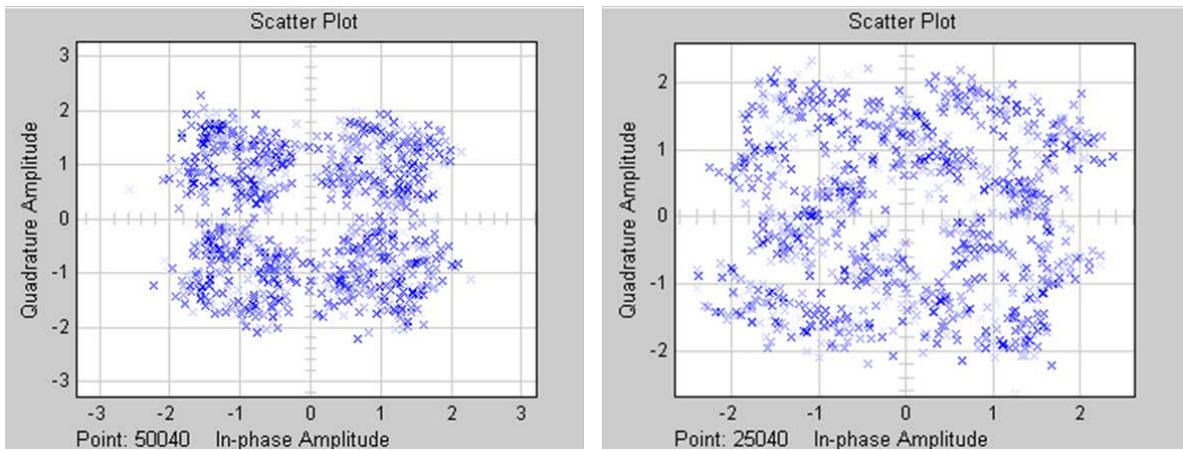


Figure 46. Constellation diagrams for I/C levels of -4 dB and -3 dB respectively.

This final test is by no means intended to confirm or refute any well researched studies in the impact of co-channel interference on a QPSK signal. However, the fact that it echoes the results of such well researched studies, such as [29], highlights its value in application towards such research.

VI. FUTURE WORK

In following the course of the research documented in the research methodology, this work successfully completed the first phase and most of the second phase of research. Additional focused study on the effect of co-channel interference on the initial demodulation of the HP signal is warranted. Further detailed analysis on the impact of LP signal interference on the HP signal needs to be completed in order to better proceed in the design of a cancellation circuit.

The next major phase of research to be conducted is the design and implementation of a cancellation circuit. The cancellation circuit should use information available from the initial demodulation of the HP signal to increase the performance of the canceller. For example, information from both of the synchronization circuits can be leveraged to enhance the quality of the HP replica signal, which will aid in its removal from the received additive sum of the HP and LP signals.

Upon successful implementation of a HP signal canceller, the LP signal demodulator can be implemented, and the performance of the demodulation of the LP signal can be studied. This study should include investigation of the practical limits of the power ratio between the LP and HP signals that support successive demodulation. Additional research can be conducted on other means to improve the performance of the cancellation circuit as a means to improve the performance of the LP demodulator. One such possibility is the use of non-linear modeling of the satellite TWTA to better replicate the HP signal replica as studied in [13],[16].

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VII. CONCLUSION

During the course of this research, we completed the incremental design of a discrete-time QPSK transmitter and receiver within the Simulink modeling environment. The receiver design incorporated the use of both a carrier synchronization circuit and a symbol timing synchronization circuit. Sufficient description of the design process was included to allow this initial design to be replicated and modified as necessary for further research. This receiver is representative of real-world receiver design. It can serve as the basis for ongoing communications research in the demodulation of layered modulation satellite communications signals, as described in the research methodology and future work chapters. It is also reasonable that this model could be used for other unrelated research.

Initial tests of the receiver show that it closely replicates the performance of the optimum QPSK receiver. Establishing better algorithms for the control loops present in the synchronization circuits is possible and would benefit future research into the design of discrete time radios. To continue research in the successive demodulation of layered satellite communications signals, additional analysis on the impact of the LP signal on the initial demodulation of the HP signal is required. The use of forward error correction codes with the above system merits exploration. It is reasonable to assume that error correction coding will increase the receiver's ability to recover the HP signal. With a better recovery of the HP signal, the signal canceller that will be developed in follow-on research will be better able to aid in the recovery of the LP signal.

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APPENDIX A. LOOP FILTER COEFFICIENTS

Loop filters were employed in both the carrier phase/frequency synchronization circuit and the symbol timing synchronization circuit. The purpose of the loop filter is to protect the synchronization circuits from erroneous measurements that result from noise in the circuit. The loop filters also characterize the responsiveness of the synchronization circuits to the presence of step or ramp errors detected between the received signal and the local oscillators. As discussed earlier, because we wish to be able to respond to both step errors and ramp errors, we need a second order loop to meet these performance requirements. A popular loop filter equation is the proportional plus integrator equation which is represented in the Laplace domain as $H(s) = K_1 + K_2 / s$ [23]. This loop equation has two constants that need to be determined for the desired performance of the loop filter, K_1 and K_2 . Additionally, to understand the associated circuit's performance requires identification of two additional constants, K_p and K_o . The parameter K_p represents the gain of the error detector, either the phase error detector or the timing error detector. The parameter K_o represents the gain of the controller, whether it be the DDS that drives the rotator in the carrier synchronization circuit or the modulo-1 timer in the symbol timing synchronization circuit [18]. The only other two parameters which define the performance of the loop filters are the damping factor ζ and the natural frequency ω_n . These two parameters define the performance of the second order response of the system, with $\zeta = 1$ representing a critically damped response (no overshoot), $|\zeta| > 1$ representing over damped systems and $|\zeta| < 1$ representing an under damped response. The natural frequency represents the frequency of the decaying sinusoidal oscillations that are present in the under-damped response. These concepts are the basics that are discussed in undergraduate electrical engineering controls curricula and may be found in an introductory text or in a text dedicated to PLLs such as [23]. Another parameter which is more useful in understanding the performance of a PLL is the noise equivalent bandwidth B_n . The noise equivalent bandwidth has been calculated for a proportional plus integrator loop to be [18]

$$B_n = \frac{\omega_n}{2} \left(\zeta + \frac{1}{4\zeta} \right). \quad (\text{A-1})$$

It is common practice in digital communications to specify the noise bandwidth relative to the symbol rate $1/T_s$ [18]. Qualitatively, the larger the time-bandwidth product $B_n T_s$ is, the quicker the PLL response, and the smaller the time-bandwidth product, the slower the PLL response. This response time translates into the number of symbols that may be received while the receiver is gaining coherency. On the other side, the longer the response time, the more immune the PLL is to the effects of noise. Overall, these two performance goals must be balanced based on the desired performance and the nature of the channel [18]. Quantitatively, the time for a PLL to lock T_{LOCK} reducing the phase error to a very small value is the sum of the time required to first match the frequency of the input T_{FL} and the time to reduce the phase error to an arbitrary low level T_{PL} . It has been shown that [18]

$$T_{FL} \approx 4 \frac{(\Delta f)^2}{B_n^3}, \quad (\text{A-2})$$

$$T_{PL} \approx \frac{1.3}{B_n}$$

where Δf is the frequency offset in Hz. The pull-in range is the range of values of Δf for which the loop can acquire lock.

With the above parameters, it has been shown that the loop coefficients K_I and K_2 for a discrete-time realization of a proportional plus integrator loop can be calculated from [18]

$$K_o K_p K_1 = \frac{\frac{4\zeta}{N} \left(\frac{B_n T_s}{\zeta + \frac{1}{4\zeta}} \right)}{1 + \frac{2\zeta}{N} \left(\frac{B_n T_s}{\zeta + \frac{1}{4\zeta}} \right) + \left(\frac{B_n T_s}{N \left(\zeta + \frac{1}{4\zeta} \right)} \right)^2}. \quad (\text{A-3})$$

and

$$K_o K_p K_2 = \frac{\frac{4}{N^2} \left(\frac{B_n T_s}{\zeta + \frac{1}{4\zeta}} \right)^2}{1 + \frac{2\zeta}{N} \left(\frac{B_n T_s}{\zeta + \frac{1}{4\zeta}} \right) + \left(\frac{B_n T_s}{N \left(\zeta + \frac{1}{4\zeta} \right)} \right)^2} \quad (\text{A-4})$$

With Equations (A-3) and (A-4) and known values of K_o and K_p , the loop filter coefficients can be readily calculated from simple algebraic manipulation. For the heuristic phase detector used in the designed receiver, both K_p and K_o are unity, greatly simplifying the calculation for the loop coefficients [18]. The gains in the timing error detectors are much more difficult. For both timing error detectors, the gains of the detectors are functions of both the roll-off factor of the pulse shapes and the received signals power. For example, in the GTED, the gain of the TED is [18]

$$K_p = \frac{4 \left(\frac{G_a}{T} \right)^2 E_{avg}}{T_s} \times \frac{1}{4\pi \left(1 - \frac{\beta^2}{4} \right)} \sin \left(\frac{\pi\beta}{2} \right), \quad (\text{A-5})$$

where G_a is the sum of all of the gains in the transmitter and E_{avg} is the average symbol energy. In order to avoid having variable loop filter coefficients, an automatic gain control (AGC) circuit is used to provide the receiver with a consistent signal strength, allowing the use of a single value of K_p [18]. The design of the receiver does not currently employ such an AGC and instead relies on the fact that in the simulation the received signal is controlled to be at unit bit energy to simplify SNR calculations. Future designs of the circuit will need to incorporate an AGC to allow a constant K_p to be used in the symbol timing loop filter for the cases when the incoming signal strength is unknown. The K_o for the modulo-1 decrementing counter is $K_o = -1$. [18]

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APPENDIX B. TIMING ERROR DETECTOR S-FUNCTION

The code for qpsktd.m a Simulink S-function used to instantiate the functionality of the TED is given below. Notice that to change between a ZCTED and GTED requires only adjusting which of three lines of code are commented out.

```
function [sys,x0] = qpsktd(t,x,u,flag)
% This S-function both calculates the timing error and maintains
% the input buffer for the TED to account for subsequent high or
% low strobe values
%
% input: u(1) is strobe, u(2) is I channel interpolator output, and
u(3)
% is Q channel interpolator output.

%function initialization code segment
if flag == 0, % 0 ==> return sizes
    %[0 7 1 3 1 0] from;
    % 0 continuous states, 7 discrete states
    % 1 output, 3 inputs, input used in output calculation, sample time
    % inherited
    % 7 states are:
    % 1 to hold initial iteration count
    % 1 to hold past strobe value
    % 4 to hold past interpolator values, 2 values per channel
    % 1 to hold TED output
    sys = [0 7 1 3 1 0];
    x0 = zeros(1,7);

%function update states code segment
elseif abs(flag) == 2, % 2 ==> return next discrete state
    sys = zeros(7,1); % initialize sys
    if (x(1) < 3) %initial processing until TED input Buffer filled
        sys(1)=x(1)+1; %sys(1) is count
        sys(2)=u(1); %sys(2) is past strobe
        sys(4)=x(3); %sys(4) is z^-2 I channel int output
        sys(3)=u(2); %sys(3) is z^-1 I channel int output
        sys(6)=x(5); %sys(6) is z^-2 Q channel int output
        sys(5)=u(3); %sys(5) is z^-1 Q channel int output
        sys(7)=0;
        %fprintf('\nCase0 %f',x(1))
    else %normal processing
        if (u(1)==0 && x(2)==0)
            sys(1)=x(1);
            sys(2)=u(1); %skip current sample, only shift strobe
            sys(3)=x(3);
            sys(4)=x(4);
            sys(5)=x(5);
            sys(6)=x(6); %TEDBuffer left with past values
        end
    end
end
```

```

    sys(7)=0;
    %fprintf ('\nCase 1')
elseif (u(1)==0 && x(2)==1)
    sys(1)=x(1);
    sys(2)=u(1); %shift strobe
    sys(4)=x(3);
    sys(3)=u(2);
    sys(6)=x(5);
    sys(5)=u(3);
    sys(7)=0;      %normal ops
    %fprintf ('\nCase 2')
elseif (u(1)==1 && x(2)==0)
    sys(1)=x(1);
    sys(2)=u(1);
    sys(4)=x(3);
    sys(3)=u(2);
    sys(6)=x(5);
    sys(5)=u(3);
%sys(7)=x(3)*(x(4)-u(2)) + x(5)*(x(6)-u(3)); %Gardner TED
    sys(7)=x(3)*(sign(x(4))-sign(u(2))) + ...
        x(5)*(sign(x(6))-sign(u(3)));           %ZCTED
    %fprintf ('\nCase 3')
elseif (u(1)==1 && x(2)==1)
    sys(1)=x(1);
    sys(2)=u(1);
    sys(4)=0;
    sys(3)=u(2);
    sys(6)=0;
    sys(5)=u(3); %stuff missing samples
    sys(7)=0;      %TEDBuffer left with past values
    %fprintf ('\nCase 4')
end
end

%function output code segment
elseif abs(flag) == 3, % 3 ==> return outputs
    %sys=0;
    sys=x(7);
    %fprintf (' %d %d %d %d %d %d
%d',x(1),x(2),x(3),x(4),x(5),x(6),x(7))
    %fprintf ('\n%d',sys)
else % all other flags return an empty set, []
    sys = [];
end

```

APPENDIX C. SUPPLEMENTAL FILES

The following files are included with this thesis to assist in replicating the results presented in this thesis and for use in future research.

Simulink Model Files:

BPSK_Model_1b.mdl – This file is the design described in Chapter IV, Section A.

BPSK_Model_2a.mdl – This file is the design described in Chapter IV, Section B

BPSK_Model_2b.mdl – This file is the design described in Chapter IV, Section B modified with variable parameters set with the associated below script file.

QPSK_Model_001.mdl – This file is the design described in Chapter IV, Section C.

QPSK_Model_2a.mdl – This file is the design described in Chapter IV, Section D with variable parameters set with the associated below script file.

QPSK_Model_5_Tx.slx – This file is the model of the completed transmitter with variable parameters set with the associated below script file.

QPSK_Model_5_Rx.slx – This file is the model of the completed receiver with variable parameters set with the associated below script file.

QPSK_Model_6_Tx.slx – This file is the model of the completed transmitter modified to generate both the HP signal and an interfering LP signal.

QPSK_Model_6_Rx.slx – This file is the model of the completed receiver with variable parameters set with the associated below script file.

MATLAB Script Files:

BPSK_Model_2b_script.m – This file sets the variable parameters of the above associated model.

QPSK_Model_2a_script.m – This file sets the variable parameters of the above associated model.

QPSK_Model_5_script.m – This file sets the variable parameters of the above associated Transmitter and Receiver models.

QPSK_Model_6_script.m – This file sets the variable parameters of the above associated Transmitter and Receiver models.

qpsktd.m – This is the script file for the timing error detector function listed in Appendix B.

BERCalc.m – This is the script file for calculating the BER in Models 5 and 6 it was generated from the BER calculator from model 2a, a version that was lost.

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